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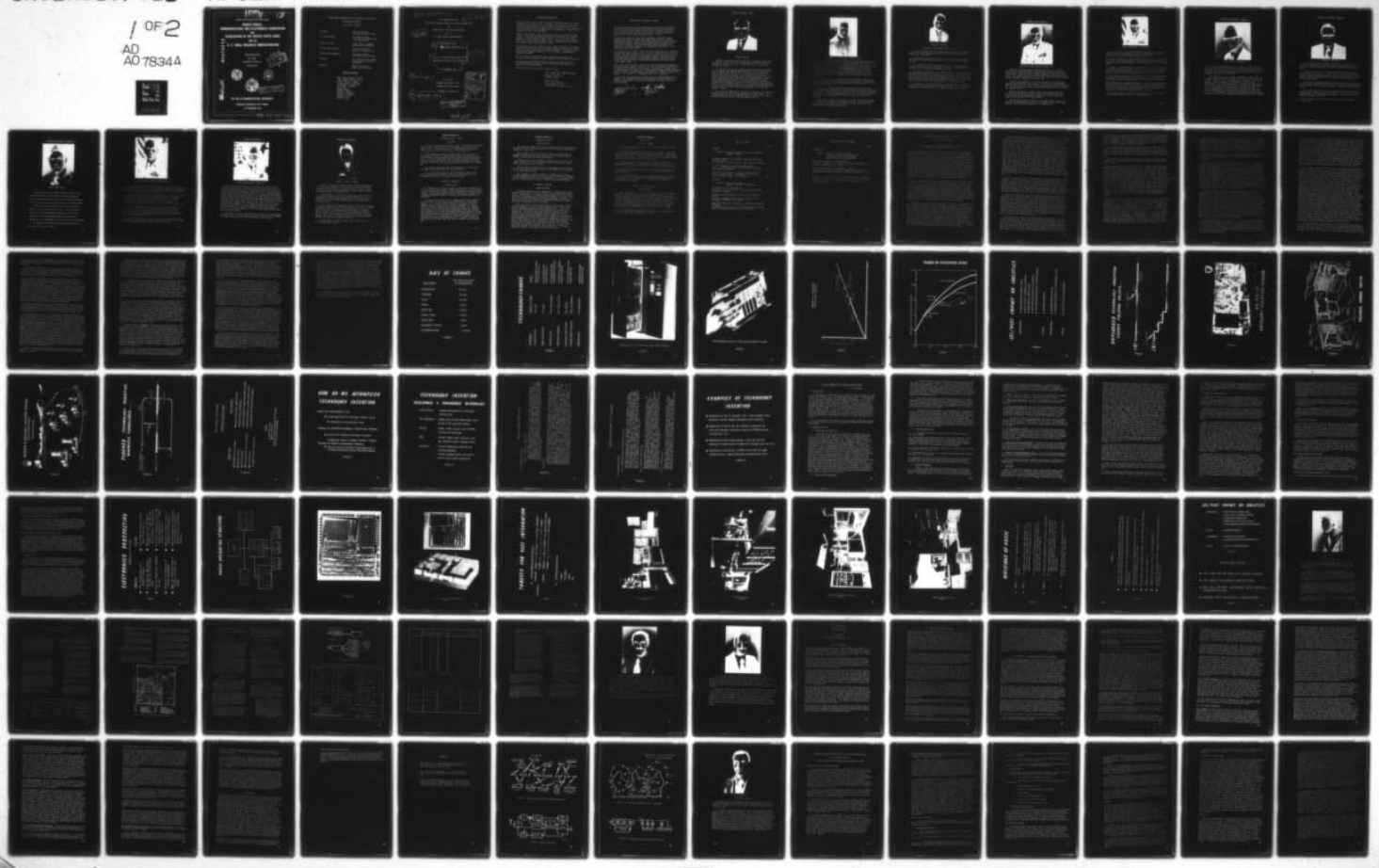

FORT MONMOUTH CHAPTERS

ARMED FORCES COMMUNICATIONS AND ELECTRONICS ASSOCIATION

AND

ASSOCIATION OF THE UNITED STATES ARMY

AND THE

U. S. SMALL BUSINESS ADMINISTRATION

PROCEEDINGS
OF THE
FOURTH ANNUAL
SEMINAR

"THE ART OF COMMUNICATIONS INTERFACES"

TECHNOLOGY INSERTION IN THE C^3I ARENA

14-15 NOVEMBER 1979

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Requests for individual copies of the papers should be addressed to the authors. Extra copies of the proceedings may be obtained from the Seminar Chairmen. Requests should include a check for $15.00 per copy, made payable to: "Fort Monmouth Chapter, AFCEA." Copies may also be obtained for a nominal fee from the National Technical Information Service (NTIS), Operations Division, Springfield, VA. 22151.

Proceedings of the First, Second, and Third Annual Seminars are available from Defense Documentation Center, Cameron Station, Alexandria, VA. 22314. The First Seminar proceedings is numbered AD-A023907. The Second Seminar proceedings is numbered AD-A044407. The Third Seminar proceedings is numbered AD-A061466.

The First Seminar covered Fiber Optics Systems and Interfaces, the AN/TTC-39 TRI-TAC Switching Systems Interfaces, and Man-Machine Interfaces.

The Second Seminar discussed Strategic Systems Interfaces emphasizing Access Area Switching Systems, Digital Tropo Modem Developments, and Tactical Data System Interfaces.

The Third Seminar dealt with RSI in the C^3I arena.

Bernard D. DeMarinis

Bernard D. DeMarinis
Technical Editor

Project Engineer
Booz, Allen & Hamilton Inc.
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Tinton Falls, New Jersey 07724

MESSAGE FROM THE GENERAL CHAIRMEN

The Fort Monmouth Chapter of the Armed Forces Communications Electronics Association and the Association of the United States Army supported by the U. S. Small Business Administration present a seminar highlighting the technology, application and field support of the newest electronic marvel, the Very High Speed Integrated Circuit - VHSIC.

The growth of technology is literally phenomenal. Equipment becomes obsolete even before it reaches operational status causing design and production nightmares. Even if the designers can keep up, the maintainers and supporters have to catch up or they face returns on equipment that they do not recognize. Thus, the problem must be articulated to all involved to provide the techniques for coping with rapid changes in the development and fielding chain.

The need for VHSIC is rapidly increasing, and we anticipate early introduction of VHSIC into military systems. It is the purpose of this seminar to present "Technology Insertion in the C3/Arena," and discuss the activities of the Electronics Research and Development Command in the design arena, the Communications Research and Development Command in the applications arena, and the Communications and Electronics Materiel Readiness Command in the support arena.

We of AFCEA, AUSA and SBA are grateful for the time and effort expended by the many committee members, speakers, and session chairmen, who were active in planning and promulgating this seminar. Also express our appreciation for their support and guidance to Lt. General Keith, Major Generals Konopnicki, Stoner and Paige, Brigadier General (P) Stubblebine, Colonel (P) Brown, and Messrs. T. A. Pfeiffer, C. F. MacDonnel and Dr. C. G. Thornton.

In particular, we appreciate the cooperation of all the attendees of this seminar. Your dialogue, discussions and comments are most valuable in improving the seminar as a forum, and suggestions for future topics will be most welcome.

Seymour Krevsky

SEYMOUR KREVSKY
CO-CHAIRMAN
AFCEA

Norman J. Field

NORMAN J. FIELD
CO-CHAIRMAN
AUSA

GENERAL CHAIRMAN - AFCEA

SEYMOUR KREVSKY

Seymour Krevsky was born on 2 July 1920 in Elizabeth, New Jersey. He received a B.S. in Electrical Engineering from Newark College of Engineering, Newark, New Jersey, in 1942 and an M.S. in Electrical Engineering in 1950.

Mr. Krevsky's career has included mobile radio project engineering with the Signal Corps Engineering Laboratories in Fort Monmouth from 1942 to 1944 and from 1946 to 1950. Mr. Krevsky was in the military service with the Army Air Corps' Air Technical Service Command at Wright Patterson Air Force Base, Dayton, Ohio, from 1944 to 1946. From 1950 to 1959, he was Chief, Microwave DF and Antenna Section of the SCEL Countermeasures Division. Mr. Krevsky joined RCA's Advanced Communications Laboratory in New York City from 1959 to June 1968 and returned to Fort Monmouth in June 1968 to the position of Deputy Director of the Engineering Directorate of U.S. Army Communications Systems Agency. Currently, he is Assistant Deputy Project Manager for DCS Army R&D Systems in USACSA.

He is a senior member of the Institute of Electrical and Electronics Engineers and a past president of the New Jersey Coast Chapter. He is a Past President of the Fort Monmouth Chapter of AFCEA and a Fellow of the American Association for the Advancement of Science.

GENERAL CHAIRMAN - AUSA

PRESIDENT, FORT MONMOUTH CHAPTER, AUSA

Dr. Field recently retired as Director of International Logistics of the U.S. Army Communications and Electronics Materiel Readiness Command after 37 years with the Army in a variety of military and civilian capacities. He received his undergraduate education at the City University of New York in Bio-physics. His graduate studies were completed at Polytechnic Institute of New York, with additional studies at Columbia University, MIT, Rutgers University, and Monmouth College. He also completed studies at the Oak Ridge Institute of Nuclear Studies, the Industrial College of the Armed Forces, and the Air Force Institute of Technology.

He served with the 63rd Infantry Division during WWII, where he was awarded the Purple Heart Medal, the Bronze Star Medal with three Oak Leaf Clusters, the Combat Infantry Badge, and the Presidential Unit Citation with Oak Leaf Cluster.

Dr. Field is a member of the American Physical Society, American Association of Physics Teachers, New York Academy of Sciences, AFCEA, ADPA, and is serving his second term as President of the Fort Monmouth Chapter of AUSA. He is listed in American Men of Science, Who's Who in the East, Who's Who in American Education, and the Dictionary of International Biography.

He has been a lecturer in the Physics Department of Monmouth College for 18 years and a member of the Monmouth Regional High School Board of Education since 1957 and its President for 9 years. He is active in numerous local educational associations.

DANIEL A. PETERSON

PRESIDENT, FORT MONMOUTH CHAPTER, AFCEA

For the past five years, Mr. Peterson has been Regional Marketing Manager for GTE Communications Products, Sylvania Systems Group, in Tinton Falls, New Jersey.

During his twenty years in industry. he has served in many engineering and marketing management positions with RCA, Motorola, and GTE Sylvania.

He received his B.S.E.E. from the University of Wisconsin and did graduate work in Electrical Engineering and Business Administration at the University of Michigan and Columbia University.

He entered the Signal Corps as a Regular Officer in 1950 after being designated DMG from the ROTC program. His seven years of service in the Signal Corps included duty as a Communications Officer in the Korean War, an Instructor in the Electrical Engineering Department at the United States Military Academy, and on two separate occasions, as an instructor at Fort Monmouth in the Officers' Department of the Signal School.

He currently is President of the Fort Monmouth Chapter, Armed Forces Communications and Electronics Association, President of the Industrial Representatives Association, and is a member of IEEE, AUSA, and ADPA.

BANQUET GUEST SPEAKER

LIEUTENANT GENERAL DONALD R. KEITH, USA

Donald R. Keith was born in Ludington, Michigan. He received a Bachelors Degree from the United States Military Academy at West Point in the class of 1949 and earned a Masters Degree from Columbia University in 1958. Among his military schools attended are the Field Artillery School, the Command and General Staff College, Armed Forces Staff College, and the Industrial College of the Armed Forces.

His key duty assignments in more than 28 years of active military service include Commander, 5th Battalion, 73d Artillery, and Commander 36th Artillery Group in Europe; Director, Research and Analysis Directorate, U.S. Military Assistance Command, Vietnam; and numerous positions on the Army General Staff.

Among his decorations, General Keith has been awarded the Legion of Merit with two Oak Leaf Clusters, Bronze Star Medal, Meritorious Service Medal, the Army Commendation Medal with Oak Leaf Cluster, and numerous foreign awards and service ribbons.

General Keith assumed his duties as the Deputy Chief of Staff for Research, Development and Acquisition on 31 October 1977 and was pinned with the rank of Lieutenant General on 4 November 1977.

LUNCHEON GUEST SPEAKER

MAJOR GENERAL EMIL L. KONOPNICKI

Major General Emil L. Konopnicki was born in Philadelphia, Pennsylvania. He enlisted in the US Army in 1945 and was commissioned from Officers Candidate School at Fort Benning, Georgia in April 1947.

He received a BS Degree from the University of Maryland, and an MBA Degree from Babson College, Massachusetts. His military education includes the Command and General Staff College, and the Industrial College of the Armed Forces.

In the 1950's he served with the 1st Armored Division and later with the 5th Infantry Division in Germany. In the early 1960's he served on the Eighth US Army Ordnance Staff in Korea, the XVIII Airborne Corps Headquarters, and the 782d Maintenance Battalion 82d Airborne Division.

In the mid 1960's he served in the Office of the Assistant Chief of Staff for Logistics, Pacific Command. In the early 1970's he commanded the 26th General Support Group in Northern I Corps, Republic of Vietnam.

General Konopnicki's subsequent assignments included Director of Supply, Office Deputy Chief of Staff for Logistics, Headquarters Department of the Army; Assistant Chief of Staff, G-4, Eighth US Army/Assistant Chief of Staff J-4, United Nations Command/US Forces Korea, and Director of Readiness, Materiel Development and Readiness Command.

He assumed his present position as Assistant Deputy Chief of Staff for Logistics, Department of the Army on 11 September 1978.

TECHNICAL CHAIRMAN -- SESSION I

DR. CLARENCE G. THORNTON

Dr. Thornton has served as Director of the U.S. Army Electronics Technology and Devices Laboratory at Fort Monmouth, New Jersey, since August of 1976. Furthermore, he is currently a consultant of the Department of Commerce on establishment and control of embargo of high technology items to the Eastern Bloc.

Dr. Thornton was born in Detroit, Michigan on 3 August 1925. He received a Bachelor of Science degree from the University of Michigan in 1949. Additionally, he received an M.S. and a Ph.D. in Physical Chemistry from the University of Michigan, in 1950 and 1952, respectively. Dr. Thornton was Director of Research and Development for the Philco-Ford Corporation for over ten years and later served as Director of Research and Engineering from 1966 until 1972. In 1972, he became Chief of the Semiconductor Devices and Integrated Electronics Technical Area, Electronics Technology and Devices laboratory, at Fort Monmouth, a position he held until 1976 when he became Director of the U.S. Army Electronics Technology and Devices Laboratory.

TECHNICAL CHAIRMAN -- SESSION II

THEORDORE A. PFEIFFER

Mr. Pfeiffer was born in Newark, New Jersey. He received a B.S. in Electronic Engineering in 1949 from the Newark College of Engineering and an M.S. degree in Industrial Engineering in 1972 from Rutgers University.

He served with the U.S. Army from October 1943 until April 1946. He entered Federal Civil Service in 1949. His first position was with the Communications/ADP Laboratory and since then he has held many positions with the Laboratory complex and the U.S. Army Electronics Command, Fort Monmouth, New Jersey.

Since 1977, he has been Technical Director of the U.S. Army Communications Research and Development Command. He exercises technical management activities directed toward developing the long-term architecture and systems.

Mr. Pfeiffer has received a number of Civil Service Awards and has written numerous technical reports and papers for the IEEE and the Armed Forces Communications-Electronics Association. He serves on all major CORADCOM Committees and Boards.

He is a member of the Board of Directors of the Fort Monmouth Chapter, AFCEA.

TECHNICAL CHAIRMAN -- SESSION III

COLIN F. MAC DONNELL

Mr. Mac Donnell has been Deputy Director of the U.S. Army Communications and Electronics Materiel Readiness Command's Logistics Engineering Directorate since its formation in January 1978 and has been serving as Acting Director since August 1979.

Prior to his current assignment, he served from 1964 to 1978 as Chief or Assistant Chief of the U.S. Army Electronic Command's Production Engineering organization. His initial assignments with the government were spent in Maintenance Engineering as a staff engineer and ultimately as a Division Chief.

Mr. MacDonnell received his engineering degree from the University of Virginia in 1950.

SESSION I CHAIRMAN

BRIGADIER GENERAL ALBERT N. STUBBLEBINE III

Brigadier General Albert N. Stubblebine III assumed his present position as Commander of the U.S. Army Electronics Research and Development Command on 20 July 1979. Prior to his present assignment, he was Commander of the U.S. Army Intelligence Center and School, Ft. Huachuca, Arizona.

General Stubblebine was born on 6 February 1930 at Fort Sill, Oklahoma. He graduated from the United States Military Academy in 1952 and was commissioned as a second lieutenant in Armor. His early assignments and approximately half of his career were with Armor units and as a chemistry instructor/professor at the U.S. Military Academy. The balance of his career has been spent in the area of military intelligence.

General Stubblebine's civilian education includes a Bachelor of Science in Engineering (1952) from the United States Military Academy and a Master of Arts in Chemical Engineering (1961) from Columbia University. His military education includes attendance at the Armor Basic and Advanced Course, the Command and General Staff College (1965), and the National War College (1971).

General Stubblebine is married to Mrs. Geraldine Murphy Stubblebine and they have two children, a daughter, Sharon and a son, Stuart. General and Mrs. Stubblebine currently reside in McLean, Virginia.

SESSION II CHAIRMAN

MAJOR GENERAL EMMETT PAIGE, JR.

Major General Emmett Paige, Jr., was born on 20 February 1931 in Jacksonville, Florida. He received a B.A. degree in Business Administration from the University of Maryland and a Master of Public Administration degree from Pennsylvania State University. He attended the Signal School, Basic and Advanced Courses, U.S. Army Command and General Staff College and the Army War College. His assignments have included project officer in the UNICOM Systems Office,1966, Deputy Project Manager for IWCS,1968, Chief Voice Network Global Management Branch, Operations Directorate DCA, 1973, Deputy Chief of Staff, Army Communications Command, Fort Huachuca, Arizona, 1974, Commander 11th Signal Group, U.S. Army Communications Command, 1975, and Commanding General U.S. Army Communications Systems Agency/and Project Manager DCS Army Communications Systems/Commander, U.S. Army C-E Engineering Installation Agency in 1976. He is currently Commander of the U.S. Army Communications Research and Development Command.

Major General Paige has been awarded the Joint Service Commendation Medal, the Bronze Star, the Meritorious Service Medal, the Army Commendation Medal, and the Legion of Merit with two Oak Leaf Clusters.

SESSION III CHAIRMAN

COLONEL(P) CHARLES W. BROWN

Colonel (P) Charles W. Brown, Director of Materiel Management in the US Army Communications and Electronics Materiel Readiness Command (CERCOM), assumed his present position in August of 1978. Previously, Colonel Brown commanded the Division Support Command, 2d Armored Division, Fort Hood, Texas.

Colonel Brown was commissioned in 1953 upon graduation from the New Mexico Military Institute, Roswell, New Mexico. He is a graduate of the Army Command and General Staff College and the Army War College, and holds a masters degree from Pennsylvania State University.

In 1975, while at the Army War College, Colonel Brown completed a research fellowship at Northwestern University, Evanston, Illinois. The results of his research, in collaboration with Dr. Charles C. Moskos, Chairman of the Department of Sociology at Northwestern, were presented in the article, "The American Volunteer Soldier: Will He Fight?", which appeared in the June 1978 issue of Military Review. The article is currently widely used as a reference work and has been published in several languages.

Colonel Brown is a member of AFCEA, ASPA, AUSA, and the Fellow-Armed Forces Society.

SEMINAR COMMITTEE

LT. COLONEL BILLIE N. THOMAS

REGISTRAR

Billie N. Thomas was born in Mason, Texas. He received a Bachelor's Degree from the United States Military Academy at West Point in the class of 1962. He earned an M.S.E.E. in 1969 from the University of Arizona, and an M.B.A. in 1974 from Long Island University.

Colonel Thomas is Director of Support Operations, U.S. Army Communications Research and Development Command, Fort Monmouth. His duty assignments include Commander, DaNang Signal Battalion, Operations Officer 37th Signal Battalion, Staff and Faculty at the United States Military Academy, Executive Officer, PM ARTADS, Commander, 5th Signal Battalion, Fort Polk, Louisiana, and Communications Team Chief, ODCSRDA, DA.

His military decorations include the Bronze Star, three awards; the ARCOM, three awards; and other service ribbons.

He is currently Secretary of the Fort Monmouth Chapter, Armed Forces Communications-Electronics Association, and Registrar and Arrangements Chairman for the Fourth Annual Seminar.

BERNARD D. DEMARINIS

TECHNIAL EDITOR

Mr. DeMarinis is a Project Engineer at Booz, Allen & Hamilton Inc. He has more than eleven years of professional experience in fiber optics, satellite communications systems, digital tropospheric systems, and ECM systems. He has been extensively involved with military inventory radio equipment assemblages and their tactical and strategic communications interfaces.

Mr. DeMarinis received his B.E.E. degree from the City College of New York and his M.S.E.E. degree from the Polytechnic Institute of Brooklyn. He is presently Vice President of Programs for the Fort Monmouth Chapter of AFCEA and was Technical Chairman of the Second Annual AFCEA Art of Communications Interfaces Seminar. Mr. DeMarinis has been an officer of the Microwave Theory and Techniques, Antennas and Propagation, and Circuit and Systems groups of the IEEE, and was general chairman of the 1976 International Microwave Symposium. He was also Technical Chairman and General Chairman, respectively, of the 1977 and 1978 AFCEA "Art of Communications Interfaces" seminars. He was Chairman of the Princeton Section IEEE and is a member of AFCEA, the Association of Old Crows, ADPA, AFA, AUSA, Tau Beta Pi, and Eta Kappa Nu.

SEMINAR COMMITTEE

BARBARA ANN FISCHER

ADMINISTRATION

Mrs. Fischer has been associated for seventeen years with the Regional Marketing Office of GTE Communications Products, Sylvania Systems Group, Tinton Falls, New Jersey.

She received an A.A. degree from the Institute of Human Affairs, Brookdale College, Lincroft, New Jersey and has continued studies at Monmouth College, West Long Branch, New Jersey.

Currently, she is Vice President for Membership and Editor of the Chapter Newsletter of the Fort Monmouth Chapter, Armed Forces Communications and Electronics Association.

She has been an active participant in the chapter's past seminars, and this year serves as Administrator for the planning and coordination of the Fourth Annual Seminar.

Mrs. Fischer was chosen as AFCEAN OF THE MONTH in April 1979 by National Headquarters and was recipient of the MERITORIOUS SERVICE AWARD in June at the National Convention in Washington, D.C. She was awarded the Fort Monmouth Chapter's 1979 DR. HAROLD A. ZAHL MEMORIAL AWARD.

DR. HERBERT S. BENNETT

LUNCHEON CHAIRMAN

Dr. Bennett received his B.S. degree and M.S. degree in electrical engineering from the City College of New York in 1938 and 1940, respectively. Additionally, he received a Masters degree in Physics in 1947 and a Ph.D. in Engineering in 1952 from the Polytechnic Institute of New York. His doctoral dissertation on the electromagnetic transmission characteristics of the microwave lens medium and its analytic model was done under the guidance of Dr. Ernst Weber.

Since 1938, he has practiced continuously in the field of communications engineering. One of his early investigations in 1940 was the analytic modeling and setting of test standards for U.S. Army field wire and for the SCR-522 (the crystal-controlled tank and vehicular command set). His work on analytic modeling of the sectoral horn is cited in the MIT Radiation Laboratory Series, Volume 10. He has practiced engineering and management both in industry and in government and has taught, on an adjunct basis, at the Polytechnic Institute of New York and elsewhere. He is a Registered Professional Engineer in the State of New Jersey and holds a National PE Certification from the National Council of Boards of Engineering Examiners. He is a Fellow of the New York Academy of Sciences and is also active in the IEEE, ASEE, NSPE, Sigma Xi, Eta Kappa Nu, and Tau Beta Pi. Dr. Bennett is presently a member of the Board of Directors for AFCEA.

SEMINAR COMMITTEE

WARREN WOLFF

EXHIBITS CHAIRMAN

Mr. Wolff is Manager of Program Development for ANALYTICS SENCOM Group at Tinton Falls, New Jersey.

He has more than eighteen years experience in systems engineering and acquisition management for defense and civil systems. He has been extensively involved in programs for command, control and communications systems for all services, military and civil air traffic control systems, weapons and public-safety communications systems.

He receive a B.E.E. from City College of New York and an M.S. in Engineering Management from Northeastern University. He has taken doctoral studies in Operations Research at New York Polytechnic Institute.

Mr. Wolff is a member of the IEEE, Human Factors Society, Society for Information Display, Air Traffic Control Association, Tau Beta Pi, and Eta Kappa Nu.

He is an active member in the Fort Monmouth Chapters of the Armed Forces Communications and Electronics Association, Association of the United States Army, Association of Old Crows, and the Industrial Representatives Association.

KENNETH J. MACDONALD, JR.

BANQUET CHAIRMAN

Kenneth J. Macdonald, Jr., Vice President in charge of the Mortgage Department, Colonial First National Bank, Red Bank, New Jersey, has served in various capacities in the Fort Monmouth Chapter of the AUSA since the inception of the Chapter as a charter member in 1966. He served as Chapter President from 1973 to 1976. Mr. Macdonald was appointed in June to a three-year term on the National AUSA Advisory Board of Directors and has been assigned to its Finance Committee. In addition, he has completed his second year on the AUSA Resolutions Committee. He was separated from military service in 1956, first Army field USAR.

Mr. Macdonald has been involved in various civic organizations and is also a former member of the Monmouth Regional High School Board of Education. He presently resides in Fair Haven.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

NEED AND METHODOLOGY FOR TECHNOLOGY INSERTION

IN EVOLVING MILITARY SYSTEMS

Dr. C. G. Thornton
Director, Electronics Technology & Devices Laboratory
ERADCOM, Fort Monmouth, New Jersey

About seven years ago, A. Toffler, in his best seller "Future Shock," discoursed on the continually accelerating change of pace in everything—in our technology, in our businesses, in our lives...in essentially everything that we do. And the reason he labelled this phenomenon "Future Shock" was as he pointed out) that most of us represent a product of a period of time that our parents lived...a time when things that represented the boundary conditions of our lives remained fairly steady over an appreciable period of time. Most people lived in the same place throughout their lifetimes; cars were built roughly the same way for a period of 10-20 years, and most new developments—in retrospect—were more evolutionary than revolutionary. Most changes were reflected against a given baseline into which we were born. And such changes were slow enough that we could deal with them as they came up, generally one at a time, with reasonable spacing between them. To continue to operate efficiently in the future, however, man would now have to adapt both his thoughts and his actions to a continually changing environment; he will of necessity encounter greater risk but also perhaps greater opportunity.

Figure 1 provides an historical perspective on the "acceleration of change" as we moved through the 19th century and approach the end of the 20th. Note that it took about 112 years from the time photography was invented until it was a full manufacturing capability; the telephone took 56 years; the radio 35 years—with dramatic shortening of time as we progressed to the present. Note, in particular, that it only took about 1-1/2 years from the invention of the concept of a MICROPROCESSOR on a semiconductor chip until these miracle circuits were being marketed and applied to equipments; today we are already into our third and fourth generations of microprocessors with markedly enhanced capabilities. The half-life of much commercial electronic equipment today is about one to two years, by which time it is obsolete in terms of available new technology which can perform far better than could be done before.

To draw closer to the military situation, I would like to narrow my focus to the changes in electronics—more specifically to changes in electronic devices that are projected for the near future by authorities in these specialties. Figure 2 identifies several of the primary hardware building blocks of our next generation military systems; we note that performance capabilities of these evolving systems will be markedly impacted by these significant device changes. For example: in this short range look to the future, computer circuits are going to decrease in size and cost, and increase in performance by factors as high as 50X or 60X with comparable orders of magnitude changes in all of the other components. Although not detailed here, similar rates of change will occur in software, architecture, data flow and distribution, and other related fields. If we narrow our focus a bit further and probe into the heart of this impressive 60X size reduction in computer circuits, we step into the dynamic world of semiconductors and its galloping technologies.

Perhaps the simplest way to provide perspective on where we are and where we're going in this context is to look first at where we were just about eight years ago. Figure 3 shows a communications type computer of about 1972 vintage, roughly equal to an IBM type 360, built for the military by RCA. The power of this computer is represented today by something akin to what is shown in Figure 4. This current equivalent package holds about 50,000 bytes of memory and will hold a million bytes by the mid-80's. The ability to provide this much processing— in a small inexpensive package—is going to dramatically change the way we even think about the concept of a computer operating in a military system. The driving force behind such change is the increasing amount of circuitry that can be placed on a single silicon chip. If we look back to about 1960 (Figure 5), the number of devices that we could put on a chip—about 1/10 of an inch on the side—doubled every year up through the present time; there is high confidence that this rate of change is going to continue right on through most of the next decade. What started out as a significant jump from 2 transistors on a chip to 4, and then 4 to 8, is now at the point where we are going literally from 60,000 transistors per chip this year to 120,000 next year, to 240,000 projected for the following year. The typical computer of the late 60's had 5 to 10,000 gates in two racks of equipment; we get that capability today on a single semiconductor chip. The cost per computational element has decreased by over 6 orders of magnitude since the early 50's. In the future, it will probably decrease by another 4-6 orders of magnitude.

Another reference point in our perspective is the changing speed of data processing. The two upper lines in Figure 6 are representative of what the largest, available scientific type of computers today will do in terms of processing "Instructions per Second." Though computers like the ILIAC, IV, CDC Star and the CRAY I will process something on the order of a million instructions per second, they dissipate kilowatts of power with attendant kilograms of weight—characteristics that make them largely unsuitable for many of our tactical military applications. In the not too distant future, these processing speeds will be brought into the realm of small tactical computer subsystems.

Much of the military's needs for high speed processing projected out to 1980-1990 falls in the area labelled "Tactical SIGINT" which represents but one example of a uniquely military application that can benefit from orders of magnitude further improvement in chip density and speed. We are projecting high speed data processing capabilities that were inconceivable a few short years ago but which are critically needed for very high speed radar and EW signal processing to handle millions of bits of information per second gathered from our countless seasors and from the hundreds—even thousands—of emitters being used by a battlefield adversary. Other applications, with almost unlimited needs for high speed signal processing include autonomous 'Fire-and-Forget' missiles, non-jammable totally secure communications and automatic target acquisition/fire control systems.

As our ability to compress our digital electronics develops in this next decade, we will see the computer as a separate entity disappearing from most of our systems and will see instead small emulators going somewhere into the main frame of the equipment to perform all the necessary computer functions. The era of the large, centralized computer with its many accessing peripherals will fade because the cost of almost unlimited computer capability ("computational plenty") in very small packages is being reduced to the point where it makes more sense to distribute this capability throughout the system (or, in the

case of the military, distribute the computational subsystem throughout interrelated battlefield systems as needed). Computational costs and the associated size and weight requirements will be such that we can even have total built-in redundancy. In a battlefield environment, such redundancy would permit our fielded equipments to degrade "gracefully" rather than catastrophically; even self-repair is not beyond consideration.

The availability and applications of these advanced products will also produce a drastic change in military logistics (Figure 7). Specifically, we project significant changes in the military maintenance and the training processes because in evolving new systems we are calling for modularity with the aim of being able to throw malfunctioning elements away rather than repair them.

Built-in tests for diagnosis and repair is a reality today—and we are calling for this feature, as applicable, in our new engineering development specifications.

The parts count (i.e., the number of discrete elements whether modules, sealed sub-assemblies, plug-in parts, etc.) is going to go down; it is conceivable that because of the low cost, we are going to see, more and more, a tendency to make single lifetime buys of all of the repair components needed for a piece of equipment at the time that we procure that equipment. Indeed, there are many pressures to do this—first, the one time buy would be most economical; second, there will be lesser quantities of these repair parts needed because of the advanced capability of the modules we are talking about; and third, the rapidly changing technology makes it preferable to "buy it now" rather than go through the difficulty of trying to duplicate the function in a new and different technology later. Indeed a lifetime supply of spare modules may be incorporated within the equipment when shipped from the manufacturer. However, there is a counter-thought here—namely, with the right computer-aided documentation at the time of the initial buy, we will be able to reprocure the function later in whatever technology exists for IC fabrication, be it five years or ten years from now, because the computer-aided documentation will document the design independently of the specific technology required to implement it.

The problem involving training of personnel for the scores of specialized electronic equipments in our growing arsenal will grow more acute if we continue the classical approach of writing training manuals in fifth grade language, coping with the stacks of them for each issue of equipment and trying to develop the training personnel and special courses for each equipment. The new technology hopefully will solve much of this problem by permitting more and more of what we are calling "embedded training"—and by that we mean a complete simulation and training capability built-in as part of the original hardware. In other words, when a soldier sits down at his radar and pushes a button which says "Teach Me," a programmed subsystem will instruct the soldier on how to use the equipment, and will provide...via simulation capabilities built into that equipment...the essentials on how to operate that equipment under operational scenarios. This is just what you can do with a computer today—push the right button and the computer on its own screen can teach you how to program that computer. The principle is the same.

Interoperability—an area in which we now have serious problems in getting our computer equipments "to talk to each other" and getting our U.S. equipment to "talk to" the NATO Nations' equipments—needs a massive effort in standardization. Can this advancing technology we described above help? If with our "computation plenty" we can make the interfaces smart enough so they can speak many computer languages and communicate through different protocols, then all of our systems can be made flexible enough to communicate with others even though they may not have been designed to have the same interfaces.

And finally, I should note that we will have the opportunity to employ greater security in our equipment, in our communications media, our data links, etc. which we could not afford before because of the high cost of the necessary equipment.

In the face of all of this technological opportunity it is perhaps appropriate to ask how we have been doing in the utilization of new technology to help the soldier on the battlefield. If we are to answer the question honestly and objectively I feel we would have to give ourselves mixed reviews. We have fielded some smart weapons, radars with advanced signal processing, and some battlefield automation and much more is scheduled for the immediate future. In other ways, however, we are not geared to realize maximum benefit from new technology and are not accomplishing it. The fact is that it commonly takes the military something like five to eight years to get a piece of major equipment from an original design into the battlefield, and this happens only if we fix the technology at the design stage and keep changes to the absolute minimum during production. Under these conditions and after 8 years (typically) we are ready to field new equipment which is literally obsolete—technologically speaking. It is obsolete in the sense that we could be fielding equipment with much higher capability at this point in time if today's technology were used rather than the technology of eight years ago.

Additional problems arise because the generalization about "freezing" our technology in development and forever thereafter living with it, is only partially true. In the real world, the equipment design doesn't stay completely frozen. No matter how much we command that we fix on a design and stay with it, pressures of change are simply too great. What happens, typically, is either of the two things that you see in Figure 8; we may go through engineering development, through DT/OT, through first production, and then discover (say) the availability of a new part that costs one-tenth as much and is ten times as reliable--and we proceed to perturb the system by jamming the substitute in. When the finished equipment now no longer meets the tests that it originally met, or something unpredictable happens, we generate delays and cost overruns at that most critical phase of the program where we can least tolerate them; the problem is eventually ironed out or a compromise made. Much of the cost of the change may be borne by the developer with lost time in production as his penalty. Changes such as these are traumatic and, as a general rule, are made under exceptional conditions.

The other thing (Figure 8) that tends to happen as you go through engineering development and get ready for production, is to redo part of the development to include a certain desirable change before you commit yourself to the production line—and there are opportunities to do this again and again as time passes; if you take all of these opportunities you never get anything out to soldiers and this leads to the user community becoming upset because the "scientists' keep the equipment in the development mill trying to make it better and better, and never get the equipment out.

And in addition to these problems of changes in the course of the development/production cycle, the laboratories keep initiating new systems because about the time a given system is ready to be fielded, there are at least three new ideas for systems based on advanced technologies which could do a better job—and so we have overlapping developments both serially and in parallel, each in turn being overcome by the advancing art. It is also frequently said that though new equipments are continually being introduced, the replaced equipment doesn't ever get taken out; this mixing of the new and old—the so-called "high-low mix"—is a sort of way for not facing up to minimizing the number and types of equipments that we're putting on the battlefield and which we have to maintain. Current needs suggest as many as 2000 additional people at the division level are required for maintaining division level equipment; the Army says they need another 15,000 maintenance personnel back at the corps level. It would seem that we are on a path of continually increasing our requirements for maintenance and logistics support and not truly coping with the growing spiral of more and more equipment and more and more support.

The collective challenge to the developer, the producer and the logistician is to provide a strategy in the life cycle plan that would permit incorporation of a technology induced change, a new functional concept or a new component or subsystem in a less painful fully anticipated and cost effective manner to significantly improve operational effectiveness without the complete redevelopment of a replacement system. To illustrate this thesis, consider the artillery locating radar (AN-TPQ-37) in Figure 9, configured in this model with a radar van and a support vehicle on the right which houses all of the computer-electronics—all of the electronics required to accept the signal information, put the information in usable form, interpret it, direct the radar, etc. This piece of equipment went to production on an expedited basis (skipping the usual engineering development phase), even though there were known areas in the design that could be greatly improved with more advanced technology; we went to production because there was high confidence that we could and would want to change those things in the near future. (For example: the transmitter tube, with only about 250 hours of MTBF—mean time between failures—along with the other low reliability components in the modulator deck provided a marginal MTBF before production.) The laboratories did proceed to develop a satisfactory new transmitter tube, and developed a new floating modulator deck (to reduce the high voltage stress on the modular equipment); and these items joined the production stream along with a self-contained, identifiable computer system, which could not as yet be replaced with any developed equivalent function (but which technology promised could be developed). The development models of the AN/TPQ-37 Artillery Locator were built with this computer as an independent entity (Fig. 10). However, by the time of first production, microelectronics technology had advanced to where the entire computer which sat on the shelf on the right could be emulated in a small, compact subsystem--actually a small number of boards that could be put in the signal processor section on the left. This was accomplished through a product improvement program (PIP) action and there was no longer an identifiable computer as such. This freed up all the space you see on the right side so that needed COMSEC equipment could be installed.

It is interesting to speculate on what can happen next. Note in Fig. 11 that one trailer is now required for each of the three mortar locating radars and also (although not shown) for each of the two artillery locating radars. It is quite likely that in several years we will be able to pull the whole signal processor out of the shelter and put it in the trailer, dispensing with the need

for a shelter for each individual radar. In other words, we will have one shelter for all the radars within that division, permitting integration of all the weapon information at the division level to where it would be most effective.

This example illustrates the two categories of technology insertion—one made in production and one made during fielding—the latter being done effectively if planned in advance. The problems of space accommodation, interfaces, plug-in opportunity, adequacy of the power source, etc., are typical parameters that can be provided for in such anticipation.

But...there's a human problem in the implementation of technology insertion, one that warrants some comment. We must acknowledge that there is a built-in "mind-set" resistance to developing and fielding equipment with a continually changing baseline. As an illustration: a Vice President of a leading systems development organization tells of his recent conversation with an Admiral in which he told him that the first two submarines to be delivered were going to contain a certain configuration of electronic equipments, but the Model #3 electronics would do a lot more, and Model #4 would have another change—all in the interest of greater performance. The Admiral's immediate reaction was, "No way!—I want every submarine in my fleet to be just like every other submarine in my fleet." I think we all recognize the thought process. The submarines might be all alike to suit his wishes, but if they are, we certainly will have lost a critical competitive edge <u>because our adversaries are not treating their systems in this fashion</u>.

The best ways and means to make technology insertion effective but painless, remains a challenge at this time...a challenge that cannot be overcome by the developer alone. The user, the tester, the developer, and the Readiness Commands must all see the advantage and work from a coordinated plan—a strategy—on how technology insertion can be best done for each system.

Let's explore some of the practical aspects of technology insertion and some of the approaches that have been tried, and some other ideas and suggestions about which we can only speculate (Fig. 12). For example, suppose that in a normal equipment development a very meaningful change can be made during production, based on a new device which is still in development but that will become available after production starts. The equipment must go through a normal DEVELOPMENT TEST/OPERATIONAL TEST (DT/OT) sequence—without the change—before it can be released for production. If the technology insertion is <u>planned</u>, then the DT/OT test has to be adequately instrumented to provide full accurate simulation data that will be applicable to testing the replacement item when it is available. The new item (the top bar) can be tested under this DT/OT simulation at the appropriate time and if it passes these tests successfully, the change would be made. A design check test may or may not be required. The DT/OT operation must be instrumented to determine the temperatures, vibration extremes, shock, and other environment aspects so that these conditions can be simulated when testing the insertion component. At the same time, the ILS package being prepared has to anticipate the future changes to be made to provide for training and maintenance modifications and subsequent reprocurement of the advanced (substituted) item.

Indeed, our logistical operations are not really set up to take such an approach at the present time—a problem that must be addressed if technology insertion is to work.

Most development, production and fielding operations now are tuned to work from a fixed baseline, with relatively few changes; follow-on improved models are designated as B, C, etc. models, or entirely new nomenclatures are devised for the more significantly changed equipments. Each of these changes involves massive paperwork, manually modified or new manuals, etc. This process appears untenable for the future; it is unlikely that we can make a change and then wait for months to staff the change through our various operations, send the documents to the printer, get the printed changes back six months later, and then finally get them into the field and into the right hands to deal with the changed item. This procedure is grossly incompatible with future generations of equipment which will be characterized by rapid changes.

The impact of technology insertion on logistics costs requires some comment. The items on the left of Figure 13 ("Added Costs") are just some of the most immediate costs reflecting the need to update the manuals, the training, the other related documentation, the first article test procedures, etc. However, in the right column, we identify the greatly reduced life cycle cost and the favorable impact on reduction of the recurring maintenance costs that are inherent in every system now being fielded. These recurring costs in the lifetime of the equipment are enormous and the modularized, compact systems we are projecting, should result in a significantly lower cost of maintenance, permit smaller numbers of parts to deal with, reduce down times, etc.

Now let's explore some of the methodologies for accomplishing technology insertion (Fig. 14). With each new system development in ERADCOM is the requirement that the bidder describe his plan for technology insertion in the bid package. It is our intention to provide the potential contractor with the opportunity for technology insertion during the development and production cycle, beginning right from the initial design. We may have to expend extra funds to develop any projected technology insertion items independent of the original planned funding. We are seeding the technology insertion effort in the components advanced development program in order to develop the better, lower cost devices and subsystems which can replace components in existing equipments at a later date. New component development will also support the product improvement program which will continue to be an increasingly important part of the total upgrading process.

Our first overtures to PLANNED technology insertion (Fig. 15) were made by including a related requirement in our procurement specifications. The stipulation required the bidder to provide a technology insertion plan. The degree to which he does this and how well he does this becomes a part of the evaluation criteria; in other words, a successful bidder is required to have a sound technology insertion plan when he submits his design, in which he takes into account the size and shape of his proposed main frame, the development of his buss structure, and the design of his interfaces so he can accept the planned technology insertion. It is not enough to generalize a projected replacement of several subsystems throughout a complex equipment; there must be a rationale and plan for such replacement if we are to truly gain the advantages without incurring the disruptions and costly perturbations of unanticipated changes.

The basic point to be made is that technology insertion must be PLANNED. Test procedures must be developed which will allow validation of a proposed replacement without repeating costly and time consuming development/operational (DT/OT) tests, and a plan must be offered as to how to handle the

related logistics problem. The bidder must identify the practical and relevant opportunities for technology insertion, including those related to simplified/better training (i.e. simulation...if required), for built-in testing, expansion of memory, etc. In the case of the SOTAS (Fig. 16), the Army asked for a technology insertion plan, required that the equipment ultimately have embedded (simulated) training and it stipulated that when any new "boxes" were developed as part of that equipment, that those boxes would have a built-in test capability so that they can identify their own problems. The SOTAS also plans on a modulator replacement, a new power source for its remote station and future modifications in its MICNS data link for increasing bandwidth.

In this first trial of a planned technology insertion operation, the technical requirements (Fig. 16) stated that the contractor will plan technology insertion in advance, and that the design should permit the insertions at appropriate times; at the same time, such changes should not introduce delays and increase the risk of giving the soldier something less than what he wants. The requirements further identified specific areas which would be impacted just by the sheer dominance of an advancing technology—so that during development, production or fielding, the Army would want increased performance, reliability, and producibility by putting new, higher technology replacements into the system. The developer is required to consider each of these stipulated areas in addition to any other areas that he himself can see as subject to practical changes that would enhance the logistic or operational effectiveness of the system. The bidder, in his response, tells the Army how he is going to deal with such technology insertion items and makes specific recommendations for mutually planned future upgrades.

The wording of our microelectronic circuits (Fig. 17) requirements clause was also changed—whereas in the past we rigidly stipulated use of parts from a qualified parts list (particularly with regard to discrete components), we now take the position that if the developer cannot work with older parts on the qualified parts list, then he can tell us what is truly needed, wanted, and available but not yet fully qualified—and where the merit of the case justifies the developer's position, we will work with the developer in making a rational decision. This is not to cater to any contractor's whims to try to get the equipment so custom designed that only he can produce it, but we will certainly work with him to incorporate new, viable technologies so that the Army can get the logistic and operational benefits from that technology and place more of the nation's advanced technology in the field. ERADCOM will insist on modular construction wherever possible in all of its new equipments for the elemental reasons that modularization promotes technology insertion.

There are certainly many examples (Fig. 18) of effective technology insertion in Army systems—it is not a totally new concept, by any means. I mentioned the changes in the AN/TPQ-37 radar; we are similarly proceeding with a planned replacement of a plasma panel on the Digital Message Device (DMD) with a new thin film flat panel display with much lower weight and power consumption. We have a planned replacement of an IR Jammer in an airborne application and at least a dozen other items in developing systems where we are "inserting" new components that were not part of the original design (or in the original production specification).

The bottom line is that we no longer can freeze the technology--we cannot stay with the classical, accepted mind-set that stipulates freezing the technology as a matter of principle. We must overcome this stereotyped approach and carefully plan toward technology insertion. One thing is certain—we will have to accept more risk in the process than we have been willing to accept up to now and be prepared to deal with that risk so that it does not impair our ability for timely delivery of equipment to the field. We must modify our requirements documents and our test procedures to accept a higher rate of change. We expect that technology insertion, in the context we are now discussing, will have a striking impact on our logistics, particularly in the maintenance and training areas. And to repeat the point made before, a practical methodology of technology insertion must be evolved by consideration of the many practical aspects involved. There are many answers that we don't have and these must be developed by the respective specialists in their fields—the users—the R&D engineer, the test teams, the provisioners, the procurement specialists, the logistician and, perhaps most importantly, by the man holding the purse strings.

Internally, we still have a great deal of missionary work to accomplish in our Training and Doctrine Command (TRADOC). our Test Command (TECOM) and our Readiness Commands. We recognize that change will not come simply, but we are committed to working the problem.

RATE OF CHANGE

DEVELOPMENT	TIME FROM INVENTION TO MANUFACTURE
PHOTOGRAPHY	112 years
TELEPHONE	56 years
RADIO	35 years
RADAR	15 years
TELEVISION	12 years
ATOMIC BOMB	6 years
TRANSISTOR	5 years
INTEGRATED CIRCUIT	3 years
MICROPROCESSOR	1-1/2 years

FIGURE 1

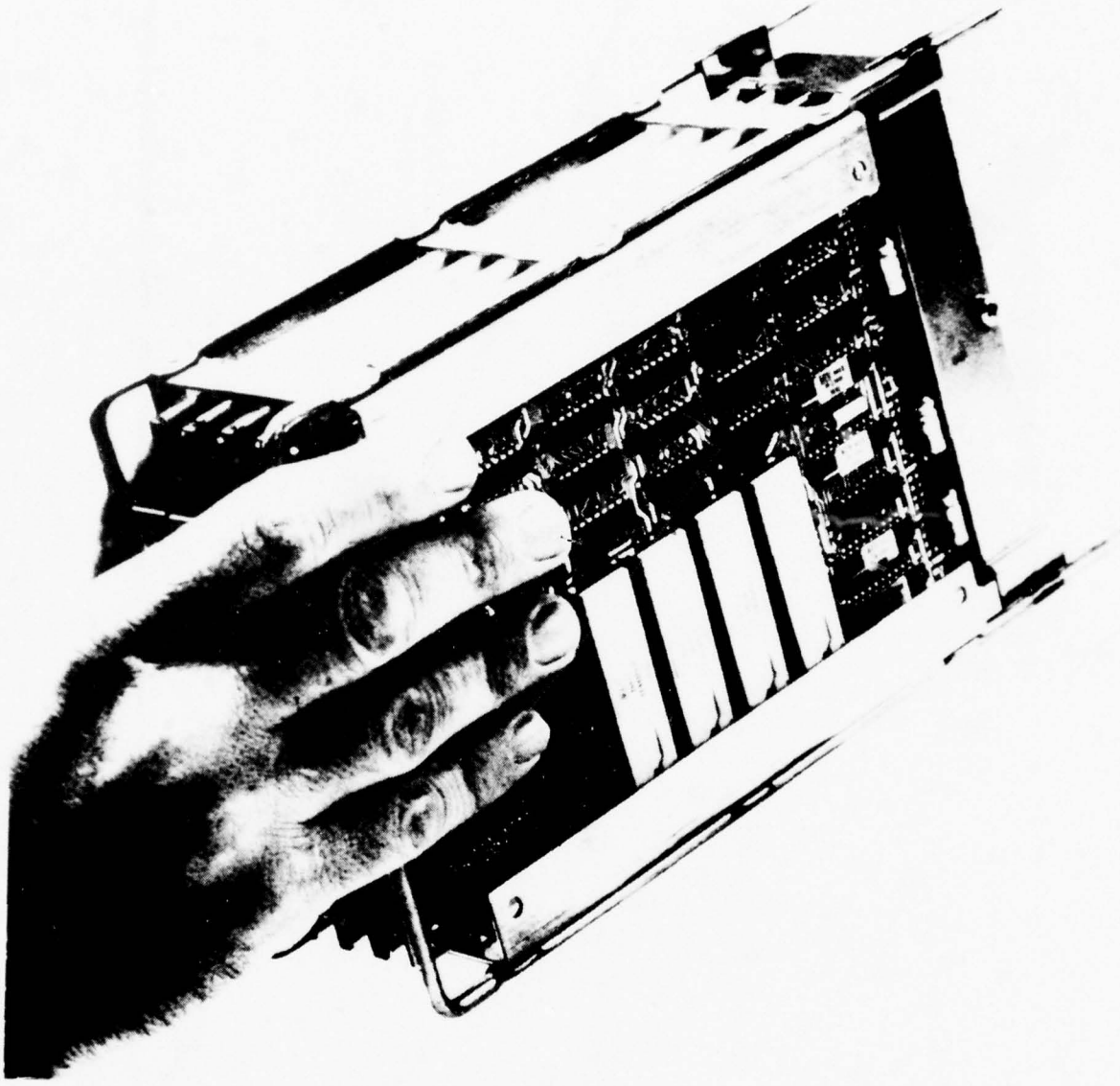
TECHNOLOGY CHANGE

TECHNOLOGY	CHANGE IN 5 YEARS	IMPACT
Computer Circuits	1/60 x size	Real-time/Highly Mobile/ C^2 Data Processing
Digital Circuit Speed	50 x speed	All Threat/Mobile EW Signal Processors
Microwave Tubes	1/20 x cost/size/power	All Threat/Affordable/ Expendable ECM Jammers
Millimeter Subsystems	1/10 - 1/70 x cost/size	Surveillance & Targeting Through Smoke/Fog
Frequency Control Devices	100 x stability	Jam Proof Nav/Comm/and Tactical Data Links
Analogue Signal Processing	1/100 x size/wt/power	
Tactical Displays	1/4 x weight/power	Lightweight Manpower Efficient Terminals

FIGURE 2

COMMUNICATIONS TYPE COMPUTER (ABOUT 1972 VINTAGE)

FIGURE 3



1979 Equivalent Version of a 1972 Communications Computer

FIGURE 4

PROGRESS IN INTEGRATED CIRCUIT LOGIC DEVICES

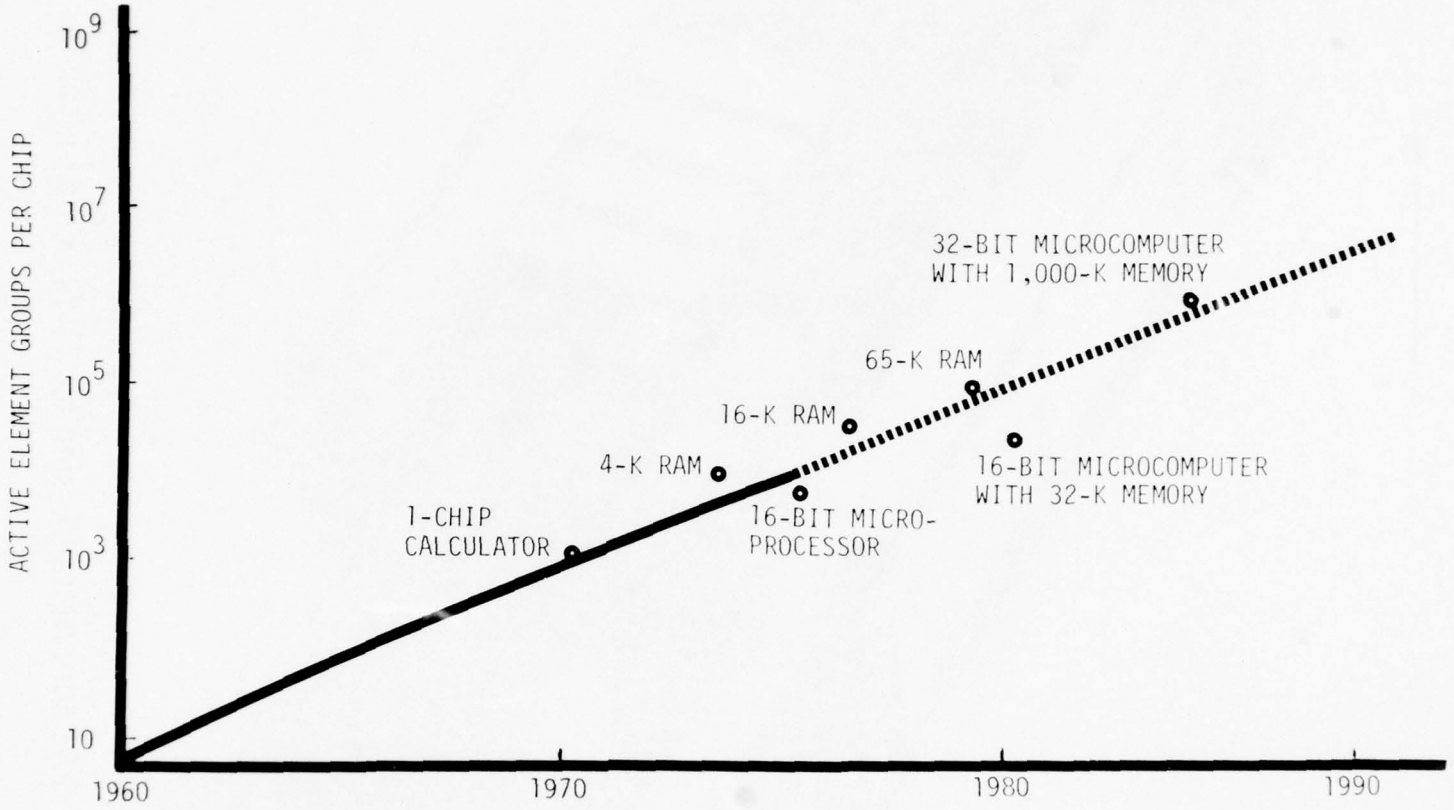


FIGURE 5

TRENDS IN PROCESSING SPEED

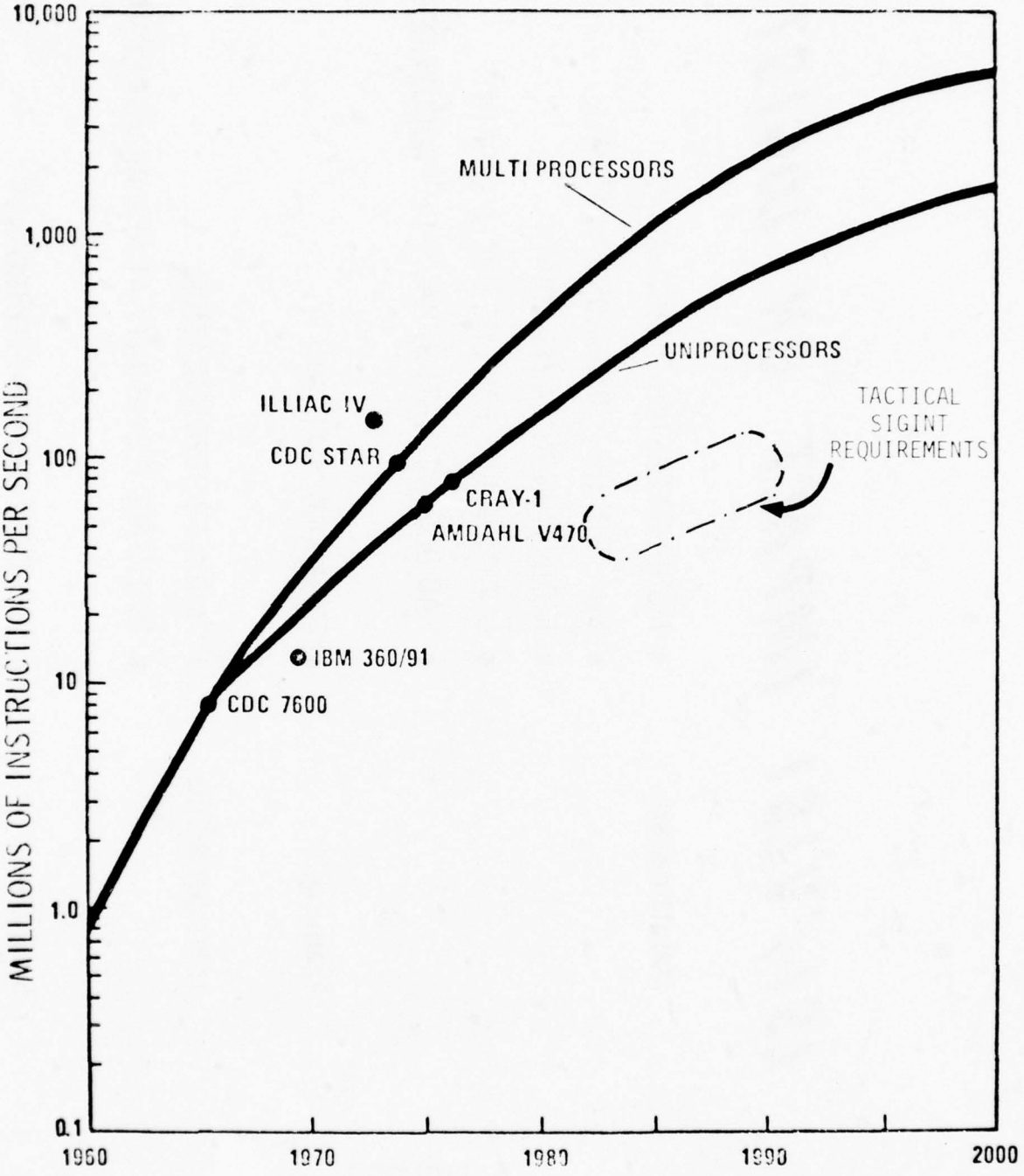


FIGURE 6

LSI/VLSI IMPACT ON LOGISTICS

Maintainability:	• MODULAR DESIGN (THROW-AWAY) • BUILT-IN TEST, DIAGNOSIS & REPAIR • REDUCTION IN PARTS COUNT • ONE-TIME BUY FOR LIFE CYCLE REPAIR • CAD DOCUMENTATION BACK-UP PROCUREMENT
Training:	• EMBEDDED TRAINING
Interoperability:	• MODULAR SPECIFICATION • INTERFACE FLEXIBILITY AT AFFORDABLE COST
Security:	• LOW COST CRYPTO-ELECTRONICS

FIGURE 7

UNPLANNED TECHNOLOGY INSERTION CAUSES FIELDING DELAYS ....

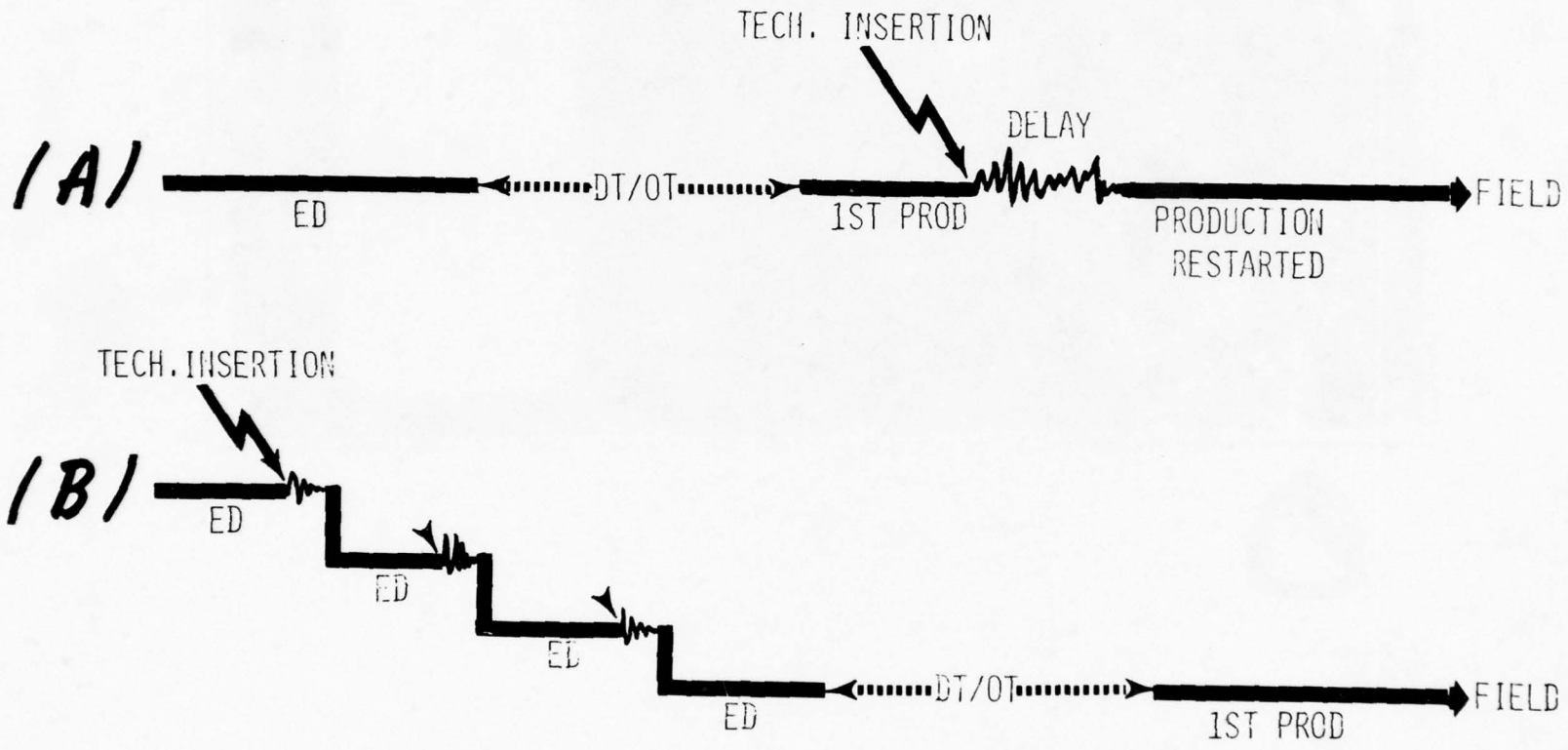


FIGURE 8

AN TPQ-37
ARTILLERY LOCATING RADAR

FIGURE 9

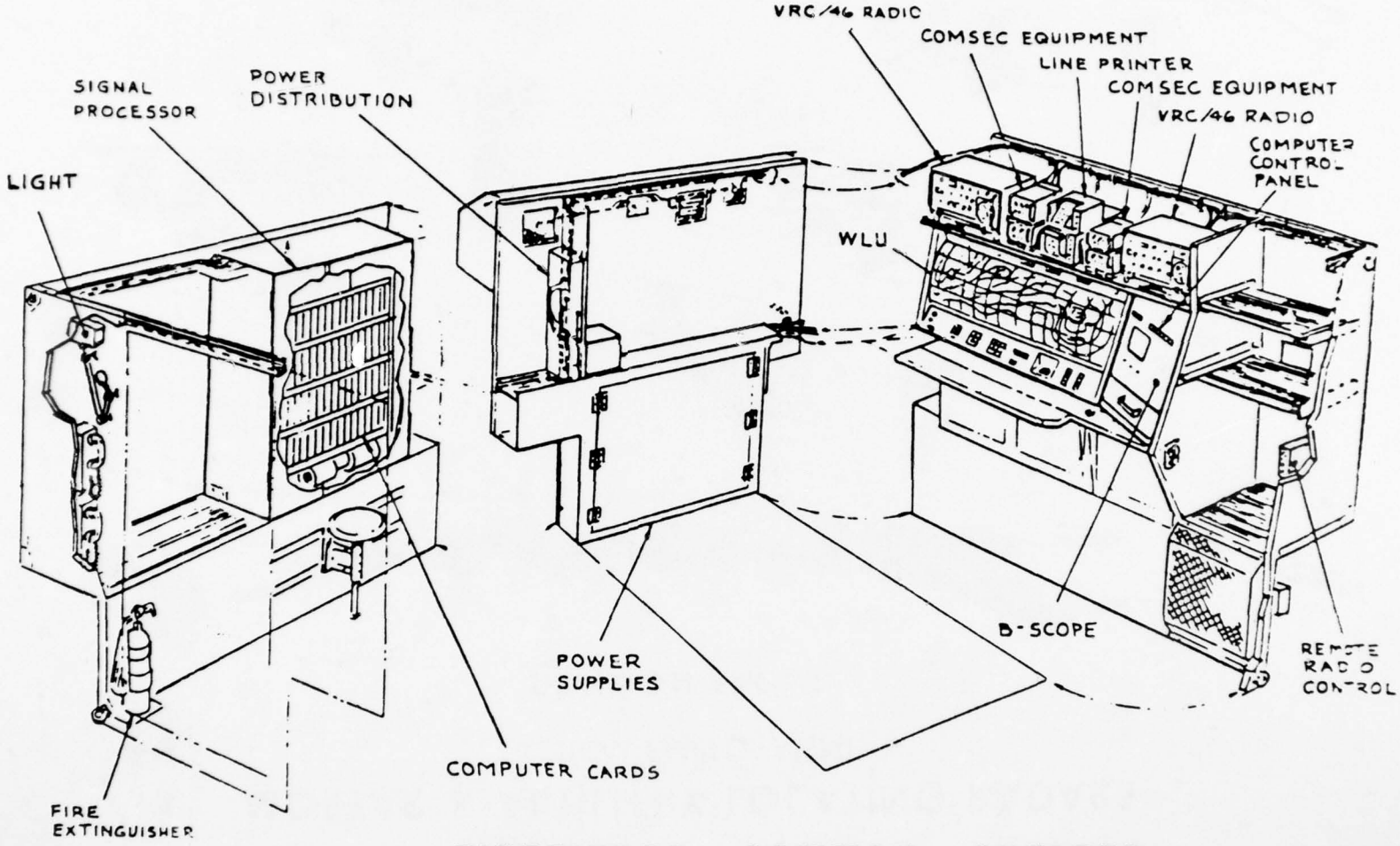


FIGURE 10

FIREFINDER COMMON SHELTER

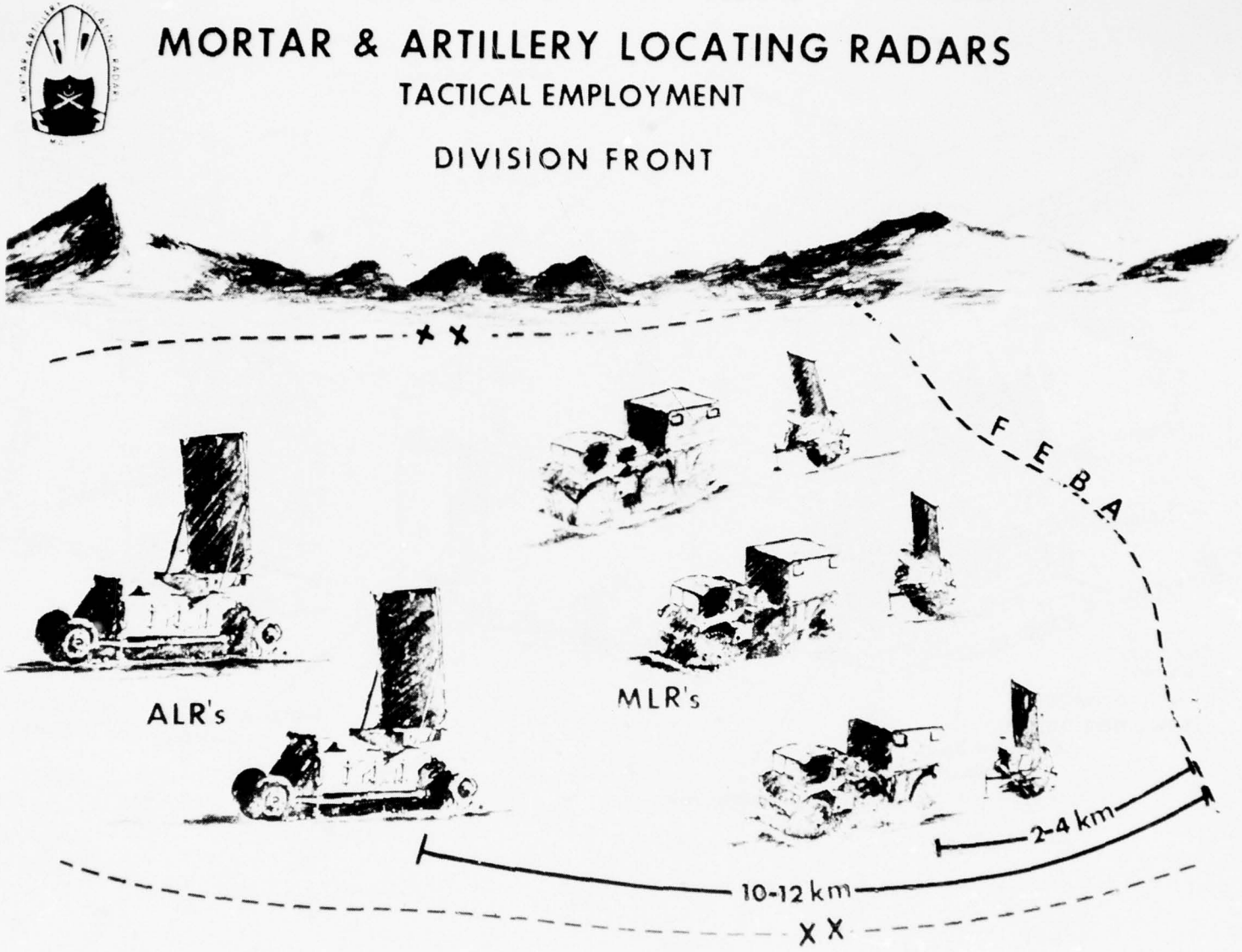

MORTAR & ARTILLERY LOCATING RADARS
TACTICAL EMPLOYMENT
DIVISION FRONT
F E B A
ALR's
MLR's
2-4 km
10-12 km
X X
X X

FIGURE 11

PLANNED TECHNOLOGY INSERTION MINIMIZES TURBULENCE ....

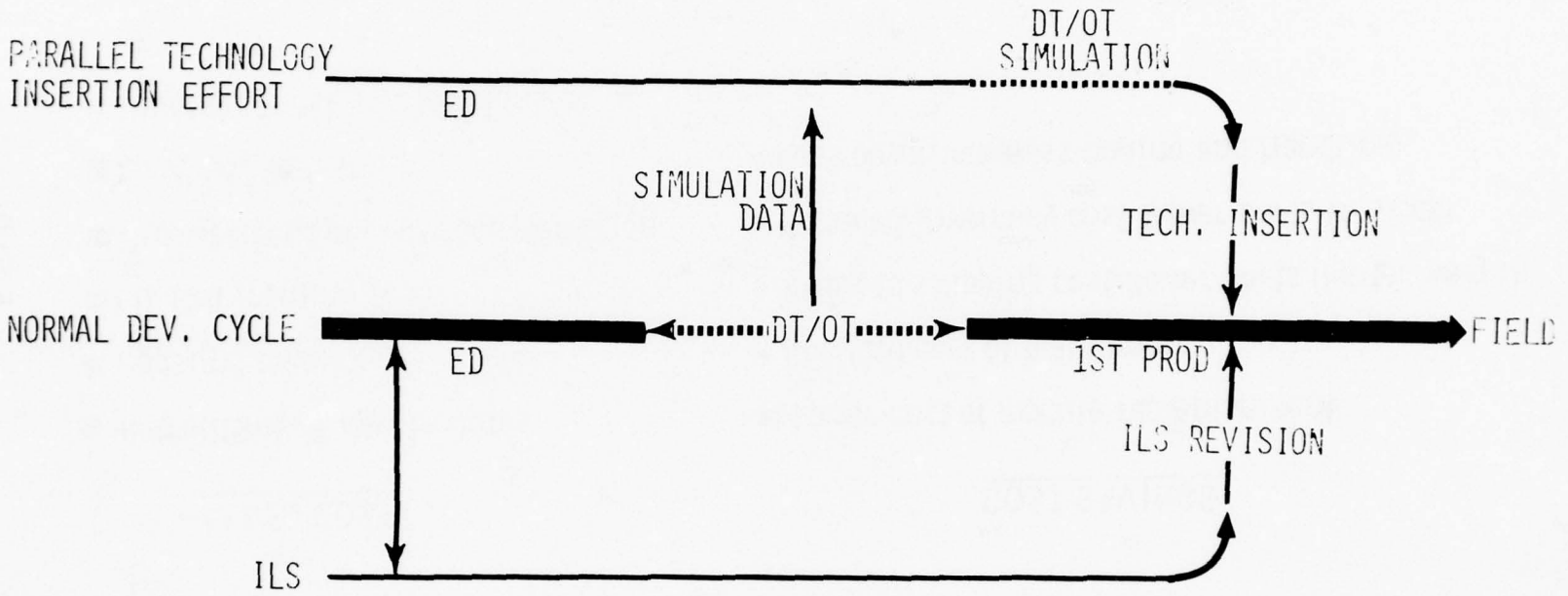


FIGURE 12

TECHNOLOGY INSERTION

IMPACT ON LOGISTIC COSTS

ADDED COSTS

- ■ Retrofitting of new modules
- ■ Updating manuals
- ■ Limited training
- ■ Procurement of CAD documentation
- ■ First article test
- ✷ Inventory cost (in stock longer)

COST SAVINGS

- ■ Lower cost of module replenishment
- ✷ Reduced cost of maintenance
- ✷ Reduced shipping cost (fewer parts, lighter weight)
- ✷ Reduced inventory cost (fewer parts in stock)
- ✷ Less downtime (less testing and handling)

FIGURE 13

Legend

✷ Recurring costs
■ One time cost
(note: comparison of cost can only be done by a life cycle cost analysis)

HOW DO WE ACCOMPLISH TECHNOLOGY INSERTION

DURING THE PROCUREMENT CYCLE:

- Provide opportunity for technology insertion during the development and procurement cycle.

THROUGH AN ADVANCED TECHNOLOGY PROTOTYPING PROGRAM

- Use the Army Advanced Technology Component Development Program to develop insertion "modules."

THROUGH THE PRODUCT IMPROVEMENT PROGRAM

- Procure, produce and install "modernization kits" or reconfigured devices/subsystems into fielded systems.

FIGURE 14

TECHNOLOGY INSERTION

DEVELOPMENT & PROCUREMENT METHODOLOGY

SOLICITATION -- Include requirement for a technology insertion plan.

BID PROPOSAL -- Bidders plan for technology growth should be part of the evaluation criteria.

DESIGN -- Design Frame, Busses, and Interfaces to accept new technology.

TEST -- Provide "design check" testing for new item validation without repeating DT/OT.

LOGISTICS -- Provide configuration flexibility with CAD documentation.

-- Provide imbedded training and built-in test for whole module replacement.

FIGURE 15

TECHNOLOGY MODIFICATIONS TO RFQ

IN THE SOLICITATION:

A.3.2.1 TECHNOLOGY INSERTION

EARLY EQUIPMENT OBSOLESCENCE IN THE FACE OF RAPIDLY ADVANCING TECHNOLOGY IS A CONCERN. CONTRACTORS WILL FORMALLY PLAN IN ADVANCE AND DESIGN TO PERMIT TECHNOLOGY INSERTION AT APPROPRIATE DEVELOPMENT/PRODUCTION PHASES TO OBTAIN SIGNIFICANT IMPROVEMENTS IN SIZE, WEIGHT, POWER, AND OVERALL LIFE CYCLE COST COMMENSURATE WITH ACCEPTABLE RISK. SUCH CHANGES CANNOT, HOWEVER, BE ALLOWED TO INTRODUCE DELAYS IN PROVIDING FIELDABLE EQUIPMENT, RESULT IN A NET ADVERSE EFFECT ON LIFE CYCLE RAM CHARACTERISTICS OR CAUSE THE EQUIPMENT TO FAIL TO MEET USER REQUIREMENTS.

IN THE BID:

A DISCUSSION OF RECOMMENDED PRODUCTION METHODS WHICH MIGHT BE USED FOR QUANTITY PRODUCTION OF THE EQUIPMENT, GIVING DUE CONSIDERATION TO MINIMIZING UNIT COSTS, INCLUDING TOOLING, DEVELOPMENT OF SPECIAL PARTS, E.G., LSI CIRCUITS, CONNECTORS, ETC., USE OF PARTS ONLY AVAILABLE FROM ONE VENDOR, ETC. A DISCUSSION OF THE APPROACH THAT THE OFFEROR PLANS TO USE TO PROVIDE OPPORTUNITY FOR TECHNOLOGY INSERTION DURING DEVELOPMENT AND SUBSEQUENT SYSTEM PRODUCTION TO FURTHER IMPROVE PERFORMANCE, LOWER COST, AND IMPROVE RAM CHARACTERISTICS (E.G., THE SYSTEM MIGHT BE DESIGNED TO PERMIT LATER REPLACEMENT OF THE GROUND COMPUTER BY A MUCH SMALLER LSI/VLSI EMULATOR). OTHER AREAS WHERE MAJOR ADVANCES ARE EXPECTED AND IN WHICH TECHNOLOGY INSERTION MAY BE CONSIDERED INCLUDE HIGH SPEED DATA PROCESSORS, DISPLAYS, ELECTRONICALLY STEERABLE ANTENNA ELEMENTS, ETC. IN EACH SELECTED AREA THE OFFEROR SHOULD PROVIDE A PLAN BY WHICH SUCH TECHNOLOGY INSERTION MAY BE ACCOMPLISHED INCLUDING CONSIDERATION OF MODULE PARTIONING, BUSS AND INTERFACE REQUIREMENTS, LOGISTICS (PARTS CONTROL), ETC.

FIGURE 16

TECHNOLOGY MODIFICATIONS TO RFQ (CONTINUED)

IN THE SPECIFICATION:

3.4.1 MICROELECTRONIC INTEGRATED CIRCUITS

MAXIMUM USE SHALL BE MADE OF INTEGRATED CIRCUITS CONSISTENT WITH OVERALL EQUIPMENT REQUIREMENTS SPECIFIED HEREIN, TO FULLY EXPLOIT THE PERFORMANCE, RELIABILITY, COST, SIZE, WEIGHT, LOGISTIC AND MAINTENANCE ADVANCES OF THESE ADVANCED MICROELECTRONIC TECHNIQUES. A FULL CONSIDERATION SHOULD BE GIVEN TO THE FACT THAT DIGITAL CIRCUIT COST AND SIZE AND DIGITAL PROCESSING SPEED WILL INDIVIDUALLY IMPROVE UP TO ONE ORDER OF MAGNITUDE DURING THE DEVELOPMENT AND INITIAL PRODUCTION OF THE SOTAS SYSTEM. SYSTEM DESIGN SHALL THEREFORE PROVIDE FOR APPROPRIATE NEW TECHNOLOGY INSERTION.

3.4.2 MODULAR CONSTRUCTION

MODULAR CONSTRUCTION SHALL BE USED TO THE MAXIMUM EXTENT FEASIBLE. THE EQUIPMENT SHALL BE SUBDIVIDED INTO BASIC MODULAR BUILDING BLOCKS AND SUBASSEMBLIES SUITABLE FOR RAPID REPLACEMENT BY INTERCHANGEABLE ITEMS OF A CORRESPONDING TYPE. IN ALL CASES THESE ITEMS SHALL BE PHYSICALLY AND FUNCTIONALLY INTERCHANGEABLE AS UNITS WITHOUT MODIFICATION THEREOF, OR OTHER ITEMS WITH WHICH THE UNITS ARE USED. MODULAR PARTIONING AND INCLUSION OF BUSS AND INTERFACE DESIGN SHALL PROVIDE MAXIMUM OPPORTUNITY FOR LATER REPLACEMENT WITH MODULES INCORPORATING ANTICIPATED NEW TECHNOLOGY TO IMPROVE SIZE, WEIGHT, POWER, AND MAINTAINABILITY.

3.4.9.1 MICROCIRCUITS

MICROCIRCUITS SHALL BE SELECTED IN ACCORDANCE WITH MIL-STD-1562. USE OF (CUSTOM NON-STANDARD) CIRCUITS SHOULD BE CONSIDERED WHEREVER SIGNIFICANT (25% OR GREATER) IMPROVEMENT IN SYSTEM OR SUBSYSTEM COST, PERFORMANCE, RELIABILITY OR MAINTAINABILITY CAN BE ACHIEVED. (CUSTOM NON-STANDARD) PARTS SELECTED SHALL BE EXPECTED TO BECOME AVAILABLE FROM TWO OR MORE SOURCES.

FIGURE 17

EXAMPLES OF TECHNOLOGY INSERTION

- Replacement of TPQ-37 "computer" with a small embedded micro-electronics emulator (between development and production).
- Replacement of TPQ-37 TWT grid modulator components with solid state modulator components having 10 X reliability (during 1st production run).
- Replacement of plasma panel display in DMD with thin-film addressed EL display having 1/3 weight and 1/4 power drain (in LRIP).
- Replacement of ALQ-144 SiC IR emitter source with BN coated graphite source to extend threat-band coverage (during LRIP).

FIGURE 18

THE VHSIC PROGRAM AND ITS IMPACT ON ARMY SYSTEMS

K. H. ZAININGER

1. INTRODUCTION.

The Department of Defense (DoD) has initiated a major new program in high speed, high throughput signal and data processing in support of the requirements for military systems in the mid-eighties and beyond. The program title is Very High Speed Integrated Circuits (VHSIC) which emphasizes its significant relationship to the technology of integrated circuits (ICs), as well as the need for higher speed processing capability. Successful completion of the VHSIC Program will enable DoD to: (1) provide critical electronic subsystems required to meet military shortcomings expected in the mid-1980s and again in the early 1990s; (2) retain and extend the US technological leadership in advanced military electronics; (3) reduce life cycle costs associated with military electronic systems; and (4) avoid a severe future problem in utilizing advanced ICs in military systems due to the fact that they will be either not available, not affordable, or both, or not meet military specifications.

It is the purpose of this paper to give an overview of the VHSIC program and to describe how the results of the program will impact future important Army systems.

2. Program Definition.

2.1 Commercial vs Military ICs.

Since there is a $6.5 billion commercial IC industry that spends 10% in IC research and development, we must ask why DoD should spend additional money in this area. The answer is simple: the commercial VLSI thrust will not meet military needs. This is because of the difference in the nature of commercial and military ICs, as shown in Figure 1. The VHSIC Program differs significantly from the broad commercial VLSI thrust in integrated circuits in at least the following respects: there will be a major emphasis on: (1) development of ICs for broad classes of military systems -- to develop technology and deliver functions for which there is no comparable commercial or industrial need; (2) achieving new architectural concepts which will minimize the need for design customization and hence reduce costs both in design, as well as in supply and logistics; (3) increasing real time system throughput which will require not only higher chip complexity, but also higher clock rates to achieve a capability for real-time signal processing; (4) military environmental requirements such as performance over a wide temperature range, radiation exposure and reliability. There will be exploitation of the higher chip complexity available to achieve a capability for built-in-test and fault tolerance with significantly improved reliability and mean-time-to-repair. While emphasis is placed on high speed signal processing applications, data processing is not excluded. All of the VHSIC efforts will take advantage of the leverage provided by the larger commercial VLSI activity, but will concentrate on those technology tasks essential to achieving military goals.

2.2 What Is the VHSIC Program?

The VHSIC Program is a joint Army/Navy/Air Force program with DoD oversight. It is a concerted THRUST -- involving the military, industrial and scientific communities -- to: (1) establish and exploit new and very promising plateaus of electronics technology on a highly accelerated basis to provide vastly expanded technological opportunities for design of low cost, high performance, high reliability military equipment; (2) provide the US Combat Arms with a significantly advanced systems capability in the 1985-1995 time frame to cope with the growing technological threat and the new dynamics of a contemporary war.

Subsystem construction and system demonstrations are an integral and key part of the VHSIC Program and are considered essential to: (1) expedite the introduction of these advanced ICs into future military systems in a timely and affordable manner; (2) provide tangible evidence of the value of the IC development to the DoD system community; and (3) realize a near-term return on the DoD investment.

The high priority subsystems to be constructed will be identified by the three services during the early stages of the program. These will include, for example, high throughput signal and data processing subsystems to be applied in systems such as military satellites, cruise missiles, fire-and-forget missiles, radar, command and control systems, wideband data communications, undersea search, electronic warfare, and signal intelligence. Subsystems/systems will be selected that allow the performance of military-related functions and missions previously precluded by computational limitations, size, weight, power and reliability considerations. The impact on Army systems is discussed in Section 5.

2.3 Key Technical Thrusts

The following summarizes some of the key technical thrusts of the VHSIC Program:

(1) New System/Circuit Architecture will be required to minimize customization and achieve such multiple application integrated circuits as: Viterbi Algorithm, Magnituding, Digital Filtering, Matrix Multiplication, Correlator, Data Sorter, Array Processor, Self-Indexing Memory, Doppler Processing, Linear Predictive Coding and Transform Encoding.

(2) Low cost computer aided design, architecture, simulation and test (DAST) of VHSIC chips will be carried out.

(3) Microfabrication techniques for high density/high speed signal processing devices will be developed.

(4) Development of reliable integrated circuits for military environments of temperature, radiation, shock and vibration with improved logistics (built-in test, fault tolerance, improved repairability) will be achieved.

2.4 Program Management.

VHSIC is a joint Army/Navy/Air Force program with DoD oversight. It is an extremely high payoff and highly visible effort with great potential to strongly impact future military, as well as commercial electronic systems. Considerable work at all levels in DoD and industry has gone into

the processes of getting the program underway. To execute the VHSIC Program such that achievement of the projected benefits to DoD can be assured, a DoD VHSIC Program Office will be established. Management will be carried out as described below in accordance with the organization charts shown in Figure 2.

1. USDR&E: The VHSIC Program is under the overall cognizance of the Under Secretary of Defense for Research & Engineering (USDR&E), (R&AT).

2. USDR&E VHSIC Coordinator: The VHSIC Coordinator will act for USDR&E on all VHSIC matters and serve as Chairman of the USDR&E VHSIC Overview Committee.

3. VHSIC Overview Committee: The VHSIC Overview Committee establishes the overall goals, objectives and priorities of the VHSIC Program. It establishes specific procedures for review and screening of VHSIC R&D tasks and assignments of task to the services for execution. It also provides the interface with USDR&E and Congress to assure adequate funding. It keeps abreast with all segments of the VHSIC and advises USDR&E accordingly.

Membership of the Overview Committee will consist of three members of each service. The service membership will consist of a representative for the Service Secretary's Offices who will act as the service spokesman on the Overview Committee, the service VHSIC program manager, and one additional service member.

4. Tri-Service VHSIC Directors: The Tri-Service VHSIC Directors exercise overall responsibility for the services for execution of the VHSIC Program through the Tri-Service VHSIC Program Office. The directors will ensure that the VHSIC Program is executed in accordance with the Acquisition and Source Selection plans. The VHSIC directors will act as the interface with USDR&E on VHSIC matters, specifically in the areas of service needs and system utilization of VHSICs.

5. Service VHSIC Steering Committee: The Service VHSIC Steering Committees are responsible for overall guidance, direction and setting of priorities within the respective service VHSIC programs and will provide the principal service inputs to the VHSIC program management office through their respective VHSIC program managers.

6. Tri-Service Program Management Office: The Tri-Services Program Management Office is responsible for the detailed planning, programming, budgeting and execution of the VHSIC Program.

The strong tri-service VHSIC management structure will effectively pull together the diverse disciplines and activities involved to execute the VHSIC Program.

3. Technology.

Now let us explore the technology thrusts of the VHSIC Program in some quantitative terms. As a reference, Figure 3 shows a Texas Instruments' microprocessor -- the type it has been selling for the last year or so, which has 27,000 transistors, 6,000 gates and is representative of today's state-of-the-art. It is logical to ask why we think this growth in high

density electronics is going to continue, or even how it is going to continue, and are there not really practical limitations rooted in the technology itself? If you take a circuit like the one at the top of Figure 4 and examine a very small cross-section, you would see that the device is made up of a number of very small elements fabricated on top of and below the surface of the silicon to form the transistors and their interconnections. Microfabrication ingenuity has made it possible to keep shrinking these dimensions year after year while at the same time making possible use of larger and larger silicon wafers from which the individual circuit chips are made. If we look at the horizontal dimensions of the conducting lines on the surface of the chip, we find that these are now (in the fabrication process) going from thousandths of an inch down into the millionths of an inch region (See Fig. 5). To date, almost all circuits with line widths of about 1/2 thousandths of an inch (0.0005") have been produced by optical techniques; we are now approaching and anticipating the usage of width dimensions as much as 100X narrower (0.000005"), dimensions which are shorter than the wavelength of light, so that we can no longer use optical processes to define them (in fact, they are too small to be seen with an optical microscope). Fabrication at this point is being accomplished by using electron beams, which have still shorter wavelengths. The extremely small vertical dimensions involved in fabricating components into the silicon surface require use of special techniques for precisely implanting desired quantities of ions into the surface. These exceedingly small dimensions bring us down to atomic dimensions; with molecular beam epitaxy techniques, we put down single atomic layers one after the other and create whatever properties we desire by selecting the atoms that we choose to implant or deposit. At the bottom of Figure 5, we cite "computer-aided design" (CAD) as an essential design tool in this new thrust into the world of microfabrication. We are now at the point where we have literally millions of elements to lay out in the design of a single computer chip ... well beyond the capacity of a human being to do by hand even in a year's time. Accordingly, both industry and the military have intensive "CAD" programs to meet their respective needs; it is almost a certainty that all of these next generation circuits will be products of such computer design (automatically laid out, fabricated, packaged, tested, etc.).

The classical picture of transistor and IC production lines with rows and rows of workers concentrated at benches processing many little chips is already changing with the advancing arts of production. Figure 6 shows an electron beam machine that automatically "writes" the complex layout patterns onto the surface: this is just one such machine developed at Texas Instruments with ERADCOM support over the last few years, and which should be in production shortly. Almost every major semiconductor manufacturer is installing this kind of advanced capability; no doubt, the semiconductor manufacturing plant of the future will look more like a super clean physics laboratory than what we typically illustrate as a manned production line.

Figure 7 shows an ion implant machine, another fabrication tool that we have had in our Fort Monmouth laboratory for three or four years, for selectively and precisely embedding impurity atoms into the surface of semiconductors.

Figure 8 shows molecular beam epitaxy equipment which allows us to put down various discrete layers of impurity atoms one atomic layer at a time.

Figure 9 shows just a small portion of a computer-aided design area where the engineers are able to sit at a console, have the computer call up all the various functions that the designer wants to perform and then have the computer rapidly integrate those functions in the desired technology into the chip layout desired.

4. Program Plan and Execution.

To meet the DoD VHSIC objectives, the program is divided into four parts called Phase 0, I, II and III, each with distinct and important goals (Fig. 10). The end goal of the entire program is to reach a capability for advanced systems performance based on an availability of ICs with submicrometer feature sizes. Phases 0, I and II will be carried out consecutively, while Phase III will be carried out concurrently with Phases 0, I and II.

Phase 0 ("Program Definition") will consist of analyses of approaches to carry out Phases I and II. It will include, for example, system and subsystem analysis, literature surveys, partitioning studies, design layouts, computer aided device modeling and such experimental fabrication and testing of device designs, layouts and processing techniques. It will result in a definitive plan and approach in the form of a proposal for the follow-on Phase I.

Phase I is conceptually divided into two parallel parts, Phase Ia and Phase Ib. Phase Ia will result in the construction of complete electronic brassboard subsystems within about four years after the start of the VHSIC Program, using VHSICs developed according to 1.25 micrometer minimum feature size with an equivalent gate-clock frequency product exceeding 5×10^{11} gate-Hz/cm^2. This replaces the conventional figure-of-merit of the power-speed product, and assumes a maximum power dissipation of about 3 watts/cm^2. A minimum clock speed of 2.5×10^7 Hz(25MHz) is a goal. Phase Ia will also result in the establishment of a pilot line production capability (not necessarily dedicated) for VHSICs with 1.25 micrometer feature sizes. It will also demonstrate the feasibility and applicability of design tools and simulation aids, and additionally, the basic principles of design/architecture/software/testing (DAST) and packaging. Phase Ib will consist of initial efforts to extend the state-of-the-art of IC fabrication and DAST to submicrometer feature sizes and associated higher gate densities. It will address broad problem areas in submicron fabrication and identify promising methods of approach. Overall, Phase I will provide the basis for further advances in Phase II.

Phase II will be driven by system requirements. It is conceptually divided into two parallel parts, Phase IIa and Phase IIb. Phase IIa will provide system demonstrations as necessary and appropriate, using the electronic brassboard subsystems constructed in Phase Ia. Phase IIb will provide a capability for further major improvements in system performance by projecting subsystem design concepts to higher performance levels and by extending the state-of-the-art of IC fabrication and DAST to submicrometer feature sizes (0.5 to 0.8 micrometers) and associated higher gate densities. The end goal for fabrication is to reach 0.5 micrometer feature sizes. Depending on the difficulty of the problem, relaxation of this goal to a maximum of 0.8 micrometer feature size will be acceptable. The equivalent gate-clock frequency product will be increased to about 10^{13} gate-Hz/cm^2. Phase IIb is considered essential to define the problems encountered in

crossing the one micrometer "barrier" established by the use of conventional optical lithography and to establish means of producing such ICs. Additionally, this part is considered essential to insure that DoD remains at the cutting edge of technology in order to meet more advanced and presently projected system needs. The possibility of constructing subsystems and providing system demonstrations with submicron chips subsequent to the sixth year of the VHSIC Program either through extension of the VHSIC Program or through separate service funding will be considered, as appropriate, later in the program.

Phase III is a six-year program, running concurrently with Phases 0, I and II, and will consist of efforts to support and supplement Phases I and II, and provide new and/or alternative directions not specifically included in them (see Fig. 11).

Phase III is considered essential to provide needed flexibility in the program, to stimulate additional innovation, and to incorporate the broadest possible group of performers. In contrast to Phases I and II, which are large integrated programs, Phase III shall consist of shorter programs of limited scope, and shall concentrate on key technologies, equipment, or tools.

5. Impact on Army Systems.

But so much for the "how we do it;" let us now dwell on the more germane topic of "what we do with it" and "what is the impact of the next generation devices in our Army applications?" As our ability to compress our digital electronics develops in the next decade, we will see high speed data processing capabilities that were inconceivable a few short years ago, but which are critically needed for very high speed radar and EW signal processing to handle millions of bits of information per second gathered from our countless sensors and from the hundreds, even thousands, of emitters being used by a battlefield adversary.

In addition to the impact that the availability of VHSICs will have on military logistics, embedded training, interoperability, and security, there will also be an order of magnitude increase in capability of our systems (Fig. 12). In order to illustrate the impact of VHSIC, four Army systems, which are expected to be major force equalizers in the 1985-1990 time frame, have been proposed as candidates to incorporate VHSIC modules and subsystems. The Army systems are listed in Figure 13.

MULTI-MODE FIRE-AND-FORGET MISSILE:

For this application, the VHSIC Program will develop an on-board processor/controller for Army multi-mode missiles (passive RF seeker, plus imaging IR or RF active seeker). This will provide product improvement with improved ECCM capability for several Army missiles (HAWK, PATRIOT, ROLAND). Also, the capability for building on-board electronic subsystems for a dual mode fire-and-forget missile will be demonstrated. These subsystems will provide high resolution imaging with autonomous target acquisition, identification and engagement in an advanced countermeasure environment.

HIGH MOBILITY INTEGRATED EW WEAPONS SYSTEM:

This application requires the development of an electronic subsystem for

emitter (target) location and identification in the microwave spectrum; and the demonstration of the capability for an EW system to be self-contained within a highly mobile (possibly expendable) RPV or ground platform which is directly integrated with available weapons systems.

BATTLEFIELD INFORMATION DISTRIBUTION SYSTEM:

Here, there is the requirement to develop an advanced electronics subsystem for real time, jam resistant, reduced intercept data/voice distribution and position location, which will incorporate PACKET RADIO, JTIDS, PLRS, and ADDS test bed concepts in an affordable manpack configuration. Also to be demonstrated is the capability for all-digital data/voice system with 10-100X improvement ECCM and LPI performance to provide jam-proof, totally secure manpack systems at throwaway cost levels.

ADVANCED TARGET ACQUISITION/FIRE CONTROL SYSTEM:

A common module subsystem will be developed for a combat vehicle FLIR acquisition/fire control system. The system will provide hands-off automatic search and multiple target handling capability under degraded visibility battlefield conditions over the full range of the XM-1 tank fire control system and will permit product improvement to airborne, anti-armor, and man-portable FLIR systems. In addition, the capability to provide the above features in a highly miniaturized version suitable for an on-board RPV system with advanced image processing to permit covert data transmission, and day/night surveillance, target acquisition, and direct weapons fire (designation) will be demonstrated.

6. Conclusions.

The VHSIC Program was initiated because the DoD judgment is that industry is not presently oriented toward meeting the military's current and future needs. However, all of the VHSIC efforts will take advantage of the leverage provided by the larger commercial VLSI activity, but will concentrate on those technology tasks essential to achieving military goals.

There will be a major emphasis on the developing of ICs for broad classes of military systems -- to develop technology and deliver functions for which there is no comparable commercial or industrial need; there will be major emphasis on achieving new architectural concepts which will minimize the need for design customization and hence reduce costs both in design as well as in supply and logistics; there will be major emphasis on increasing real time system throughput which will require not only higher chip complexity, but also higher clock rates to achieve a capability for real-time signal processing; there will be major emphasis on military environmental requirements such as performance over a temperature range, radiation exposure and reliability. There will be exploitation of the higher chip complexity available to achieve a capability for built-in-test and fault tolerance with significantly improved reliability and mean-time-to-repair. While emphasis is placed on high speed signal processing applications, data processing is not excluded. As a result of these efforts, the VHSIC Program will provide the enhanced capability needed in our systems to be able to better meet the threats projected for the mid-1980s and beyond.

ELECTRONICS PERSPECTIVE

COMMERCIAL Vs MILITARY

COMMERCIAL	MILITARY
■ HIGH VOLUME/LOWEST COST (GENERAL PURPOSE)	■ LOW VOLUME FOR SPECIFIC EQUIPMENTS (HIGH QUALITY)
■ FUNCTIONS ARE INDIVIDUALLY DESIGNED FOR VOLUME PRODUCT LINES	■ REQUIRES LOW COST CAD AND/OR COMMONALITY IN FUNCTIONS (NEW ARCHITECTURES A PRE-REQUISITE)
■ SPEED OF COMPUTATION TEMPERED BY COST	■ HIGH SPEED COMPUTATION (REAL-TIME SIGNAL PROCESSING) IS A COMBAT-CRITICAL CAPABILITY
■ OPERATION IN CONTROLLED OR LIMITED ENVIRONMENTS	■ OPERATION IN RUGGED, TYPICALLY UNCONTROLLED ENVIRONMENTS
■ DOWN-TIME CORRECTIONS MADE BY TRAINED, AVAILABLE TECHNICIANS	■ DOWN-TIME BORDERS ON INTOLERABLE (SELF-DIAGNOSIS & OPERATOR REPAIR BY MODULE REPLACEMENT ESSENTIAL)

FIGURE 1

VHSIC OPERATING STRUCTURE

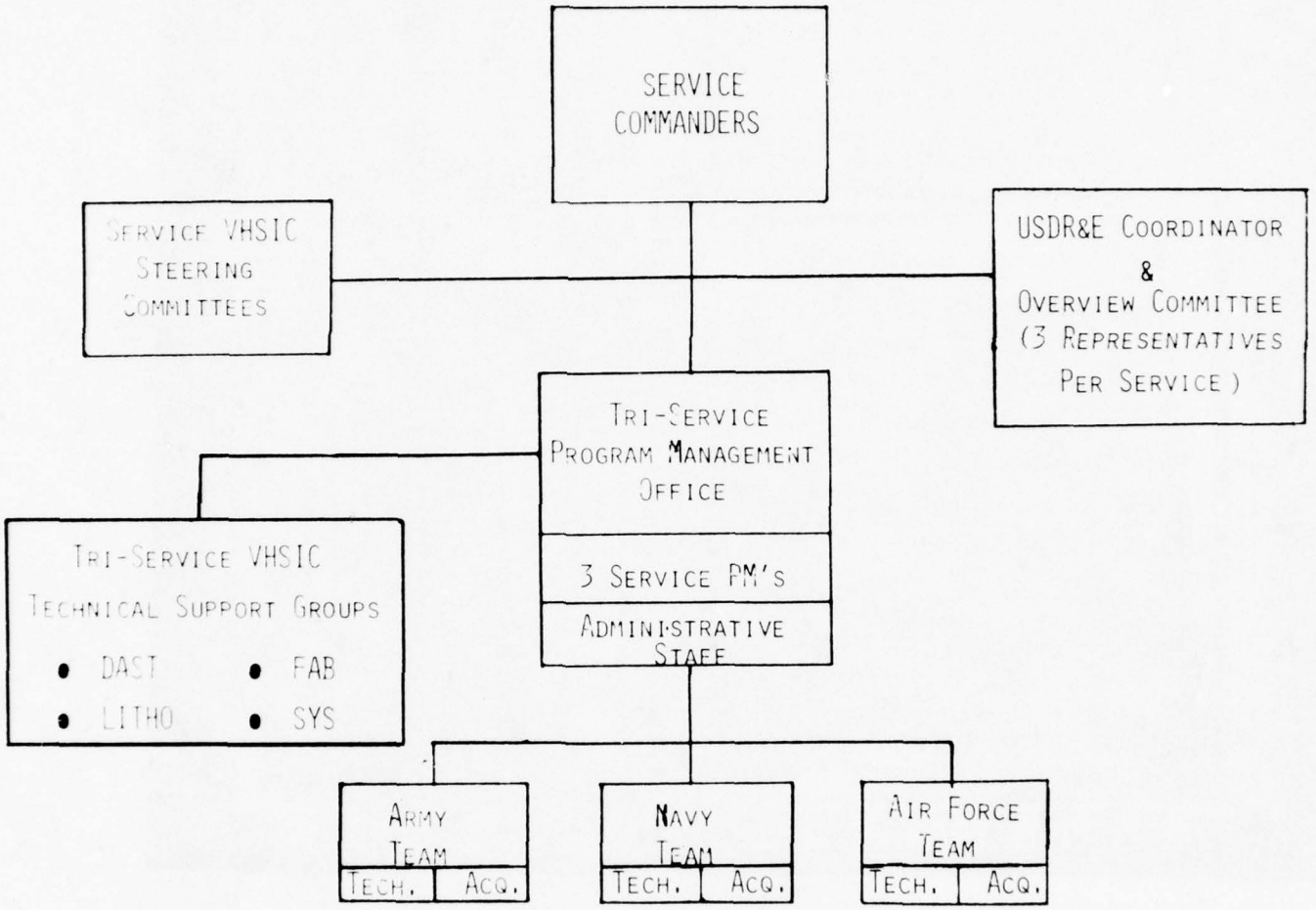
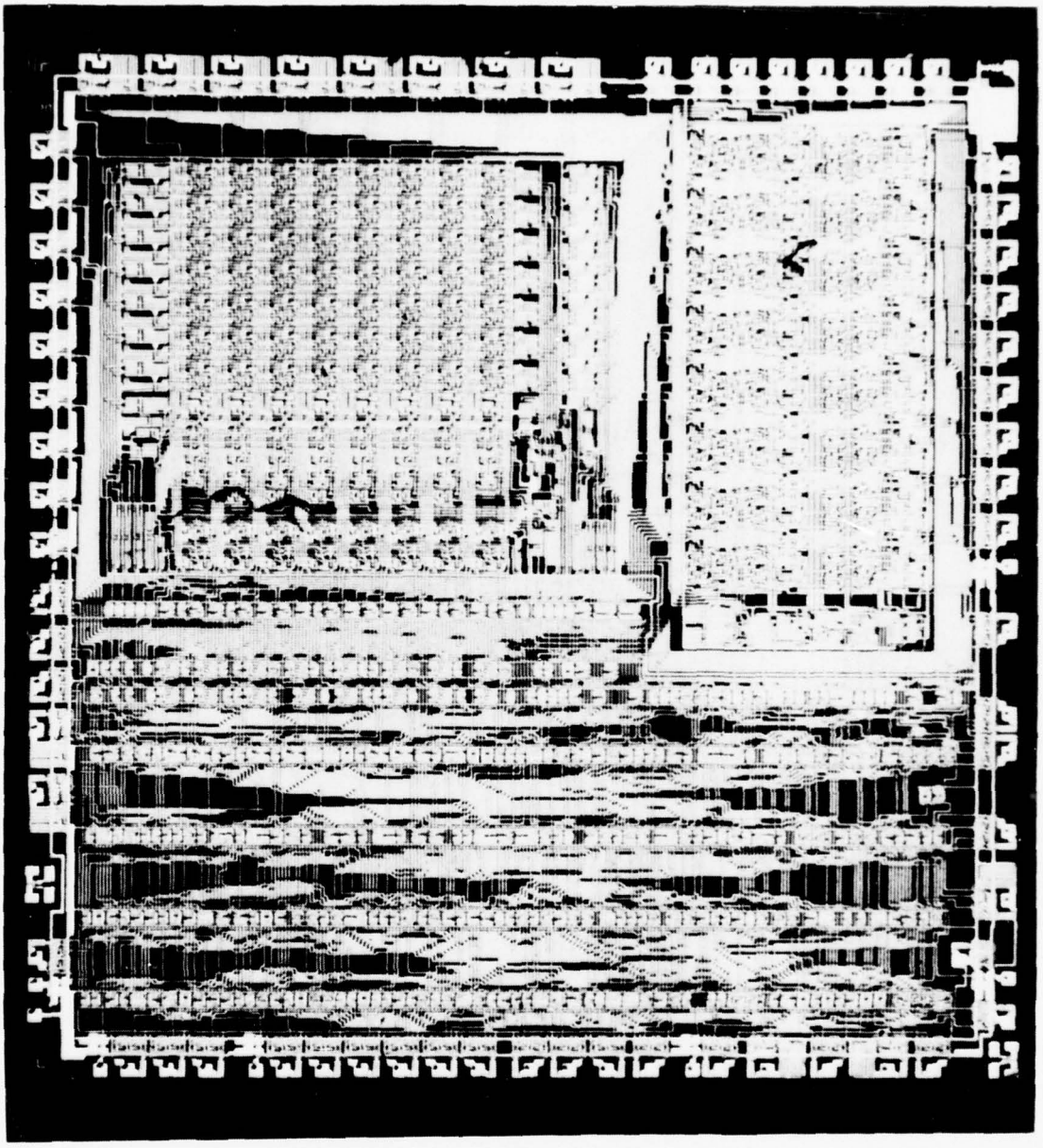
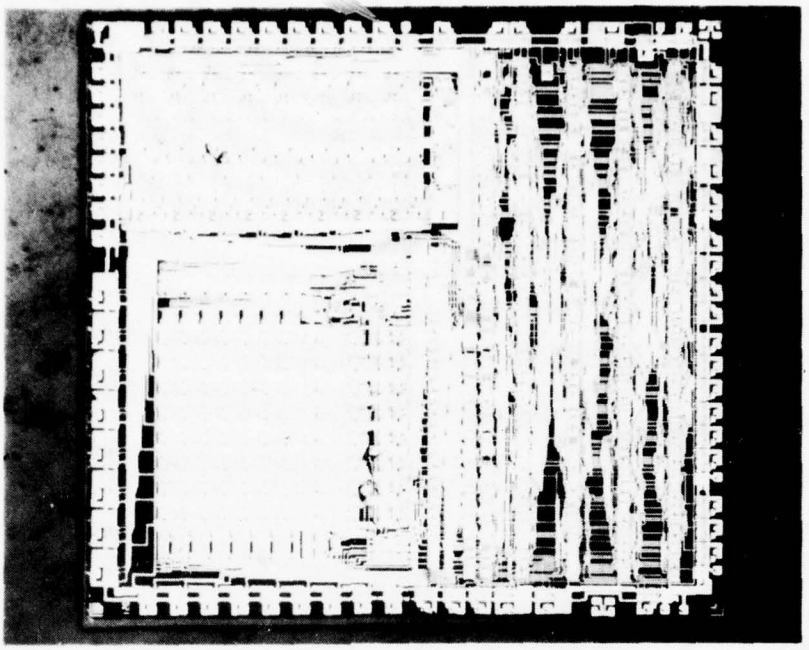
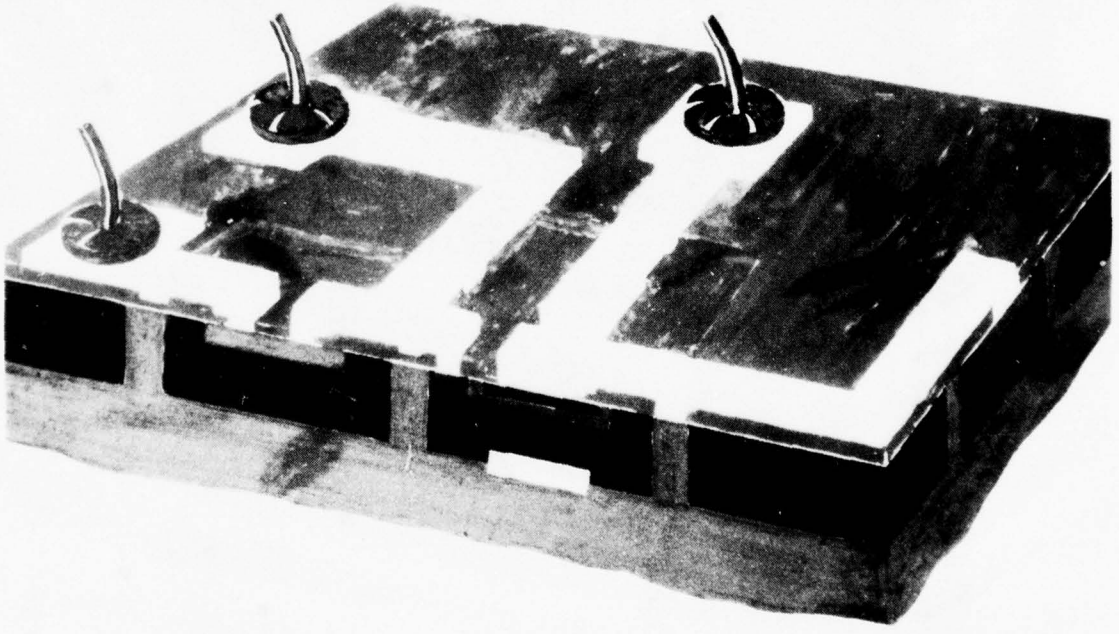


FIGURE 2



Microprocessor
FIGURE 3





Microprocessor with Cross-Section
FIGURE 4

THRUSTS FOR VLSI INTEGRATION

- MICRO-FABRICATION TECHNOLOGY

Dimensions

Horizontal: Optical → E-Beam → X-Ray Lithography

0.0005" → 0.000005"

Vertical: Diffusion → Ion Implant → Molecular Beam Epitaxy

0.00005" → 0.00000005"

- COMPUTER AIDED DESIGN

  Design

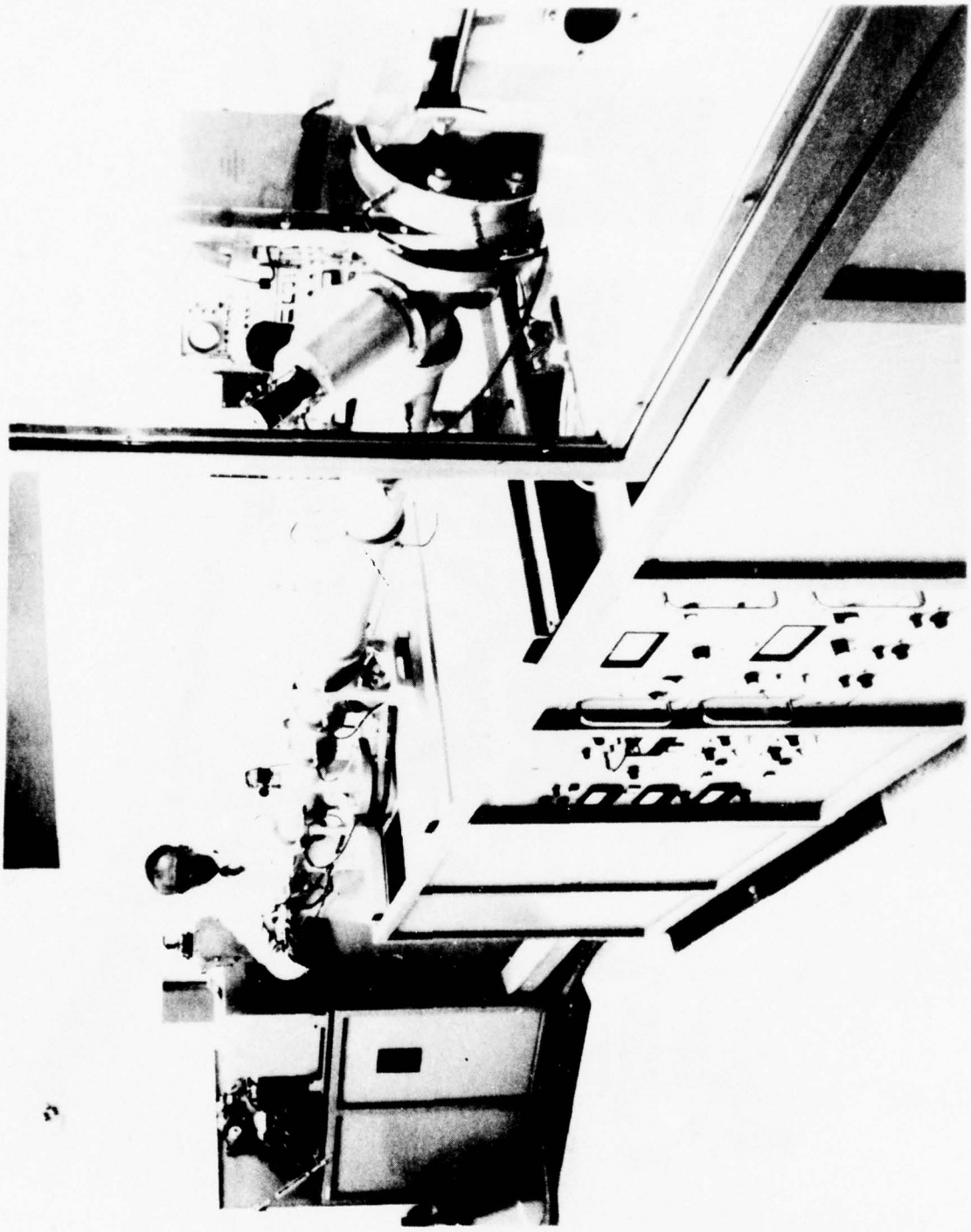
  Simulation

  Layout

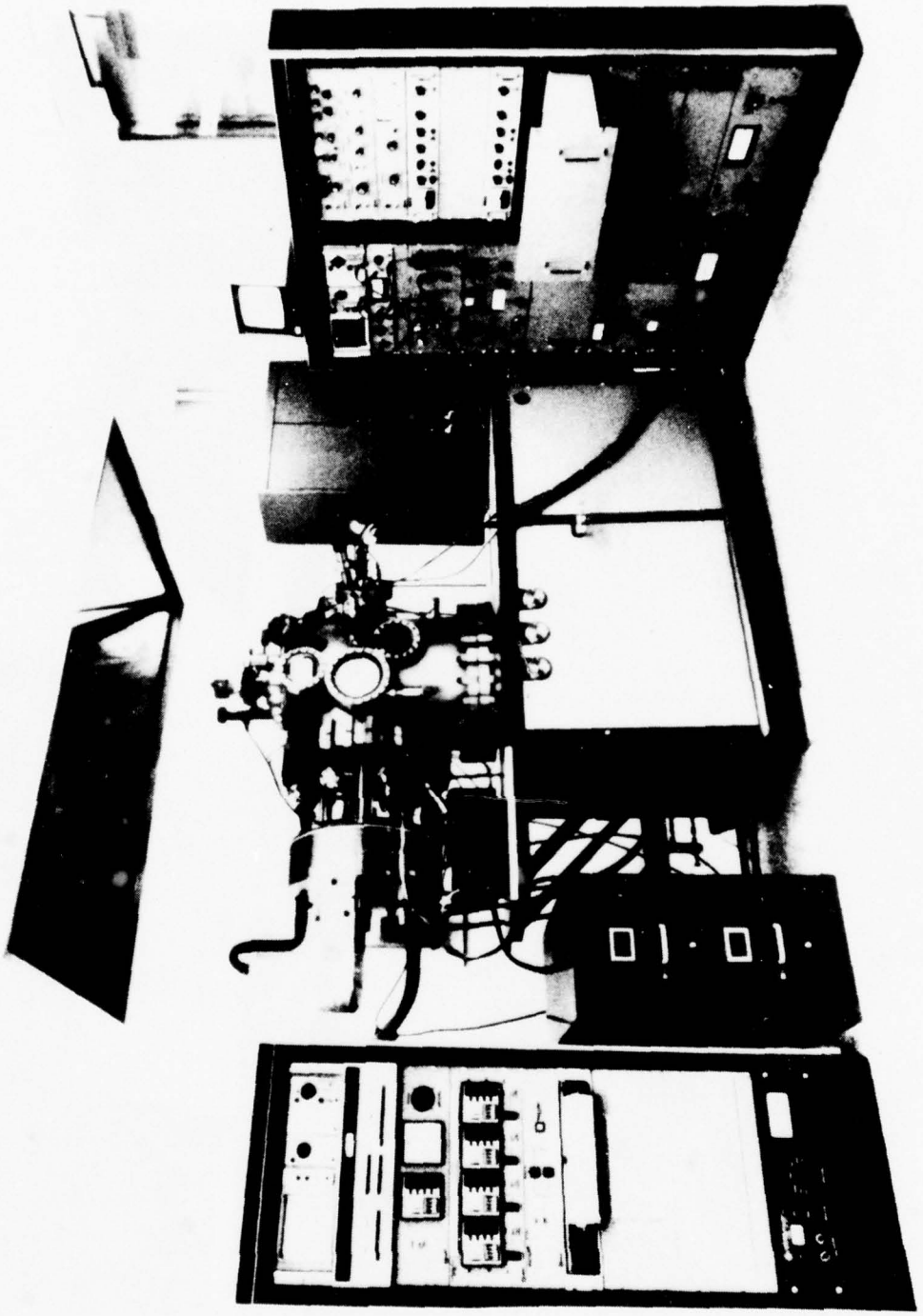
  Test

FIGURE 5

Electron Beam Machine
FIGURE 6



Ion Implant Machine
FIGURE 7



Molecular Beam Epitaxy Equipment
FIGURE 8

Computer-Aided Design Area
FIGURE 9

DIVISIONS OF VHSIC

- PHASE 0: Program definition - Analyses of approach to Phase I and II.
- PHASE I:
  - A) Construct complete electronic brassboard subsystems within 4 years using VHSICs with 1.25 μm minimum feature sizes & establish IC pilot line.
  - B) Initial effort to extend state of the art of IC fabrication & DAST to submicrometer feature sizes and associated high gate densities.
- PHASE II:
  - A) Provide system demonstrations with Phase I brassboards.
  - B) Project subsystem design concepts to higher performance levels and extend the state of the art of IC fabrication & DAST to submicrometer (0.5 - 0.8 μm) feature sizes.
- PHASE III: Provide specialized technology developments supportive of the thrusts of PHASE I and PHASE II.

FIGURE 10

PHASE III

- INNOVATIVE ARCHITECTURAL AND DESIGN CONCEPTS FOR BOTH IMPROVING THE PERFORMANCE AND REDUCING THE COSTS OF MILITARY CIRCUITS AND SUBSYSTEMS.
- ADVANCED HIGH RESOLUTION LITHOGRAPHIC EQUIPMENTS & RELATED MATERIALS AND PROCESSES.
- INNOVATIVE APPROACHES TO IMPROVING THE UTILITY AND SIMPLIFYING THE USE OF VHSIC TECHNOLOGY BY SYSTEM USERS.
- DEVELOPMENT OF NEW STRUCTURES & CONCEPTS FOR HIGH SPEED SIGNAL PROCESSING.
- INNOVATIVE TESTING CONCEPTS.
- INNOVATIVE CAD CONCEPTS FOR SELF TESTING CAPABILITIES.
- TECHNIQUES FOR DOCUMENTING VHSIC TECHNOLOGY FOR MAXIMUM AVAILABILITY AND TRANSPORTABILITY.

FIGURE 11

LSI/VLSI IMPACT ON LOGISTICS

Maintainability:	• MODULAR DESIGN (THROW-AWAY) • BUILT-IN TEST DIAGNOSIS & REPAIR • REDUCTION IN PARTS COUNT • ONE-TIME BUY FOR LIFE CYCLE REPAIR • CAD DOCUMENTATION BACK-UP PROCUREMENT
Training:	• EMBEDDED TRAINING
Interoperability:	• MODULAR SPECIFICATION • INTERFACE FLEXIBILITY AT AFFORDABLE COST
Security:	• LOW COST CRYPTO-ELECTRONICS

FIGURE 12

PRIORITY ARMY SYSTEMS

- MULTI-MODE FIRE-AND-FORGET SELF-TARGETING MISSILES.
- HIGH MOBILITY INTEGRATED EW WEAPONS SYSTEMS.
- REAL TIME, JAM PROOF, INTEROPERABLE SECURE DATA/VOICE DISTRIBUTION SYSTEMS.
- AUTOMATIC TARGET ACQUISITION IR SENSOR SYSTEMS.

FIGURE 13

BIOGRAPHY

DR. KARL H. ZAININGER

Dr. Zaininger received the BEE (magna cum laude) from City College of New York in 1959, and an MSE in 1961, an MA in 1962, and a PhD in Engineering Physics in 1964, all from Princeton University.

He joined the technical staff of RCA Laboratories in 1959 and was involved in research on silicon-based MOS devices since their original inception. In 1968, he became Head of Solid State Device Technology and since 1972 he was in charge of RCA's CCD research. From 1976 to 1977, he was Task Force Leader for RCA's LSI Technology Transfer effort.

In 1977, he joined the Solar Energy Research Institute (SERI) as Director of the Commercialization Division and, in 1978, he joined the Electronics Technology and Devices Laboratory, U.S. Army Electronics Research and Development Command (ERADCOM) as Director of the Microelectronics Division. He was involved in the planning of DoD's VHSIC Program since its inception and is presently the Army's VHSIC Program Manager.

Dr. Zaininger was Editor of IEEE Transactions on Electron Devices (1977-79), is a Fellow of the IEEE, and is Visiting Professor at the Hebrew University of Jerusalem.

INSERTION OF VLSI/VHSIC INTO SIGNAL PROCESSING SYSTEMS

K. Nummedal, C. T. Brodnax, W. H. Evans,
W. L. Smithhisler, P. R. Hart

ABSTRACT

The issues of technology insertion in signal processing systems are defined. Motivations for and means of insertion are outlined. This strategy is based on Hughes experience with existing Army ground systems (TPQ 36/37) and avionics systems (AN/AWG-9). It is shown that planning for technology insertion during the advanced development phase is a key element of the strategy. Advanced technology can provide a reduction of LCC in addition to providing improved performance. Advanced DoD signal processing systems currently in the planning stages are shown to drive the performance requirements and hence the need for LSI/VHSIC technology development. In these cases insertion is automatic because system feasibility depends on the availability of advanced technology.

TECHNOLOGY INSERTION IS A FAMILIAR CONCEPT

Replacing or upgrading systems by utilizing new technologies has been a common practice in the defense industry for many years. Hughes has found that the insertion of new technology into existing avionics systems can be accomplished if the new technology offers sufficient advantages in terms of 1) reduced cost of production, 2) increased capability of the equipment, 3) improved reliability and maintainability and 4) reduced volume and weight. Major technology changes in existing Hughes systems have occurred for all these reasons. Examples are given in Table 1.

In some cases, such as the F-15 Radar, the cost of insertion was paid for by savings on forward production costs. In another case, where production was completed with the MA-1 fire control system, cost of insertion was paid for by reduced maintenance cost of the existing equipment. In general, Hughes has found that, in addition to offering one or several of the above advantages, a new technology should be a) well developed, b) in production, c) multiple sourced, and d) adaptable to change. If it meets these criteria, its chances of acceptance are high.

Given that the task of technology insertion is well understood, what are the specific problems of introducing VLSI technology?

VLSI TECHNOLOGY INSERTION PROBLEMS

The use of Large Scale Integrated Circuits (LSI) and Very Large Scale Integrated Circuits (VLSI) in military equipment is currently lagging the use in commercial equipment. Explanations for this lag are given in references (1 and 2). Major deterrents to technology insertion are:

1. A large number of military systems require high speed signal processing that cannot be provided with commercially available microprocessor chips.

2. Long Lead time, high development risk and front end development cost for LSI and VLSI circuits - particularly for custom LSI and VLSI - have traditionally discouraged program managers when lower risk alternatives exist.

3. The DoD semiconductor market is only 7 percent of the total semiconductor market. The DoD leverage of new LSI developments in semiconductor companies is therefore limited.

4. Special requirements such as radiation hardening and military temperature range (-55°C to +125°C) limit the technology options.

5. Military qualification of parts in accordance with MIL-M-83510, and MIL-STD-883 for the Government qualified parts list (QPL) increases cost and delays introduction of new parts to the user.

6. Lack of reliability data and pessimistic predictions for LSI based on MIL-STD-217B reliability handbook delays introductions into systems.

7. Lack of standardization (except for MIL-STD-1553 interfaces, Navy SEM modules, and a few other examples) leads proliferation of part types. This proliferation reduces production quantity for each part type, in direct violation of the "Law of high volume" adhered to by most semiconductor companies.

Table 1. Examples of Technology Insertion into Existing Systems

Program	Subsystem	Old Technology	New Technology	Time Frame	Motivation/ Justification
F-106 MA-1	Fire Control	Vacuum Tube	IC Computer	1966-1970	Improved Reliability and Maintainability
F-15 APG-63	Radar Data Processor	Core Memory	EAROM Solid State Memory	1978-ongoing	Reduced Cost Increased Capacity
F-14 AN/AWG-9	Central Computer	Thin Film Memory	14-Mil Core Memory	1980-on	Reduced Cost Increased Capacity

8. Software costs tend to dominate hardware cost; hence the system cost impact of LSI may be insignificant.

9. Life cycle cost (LCC) payoff using LSI and VLSI is generally not quantified. Further analysis may provide guidance as to what the real cost drivers are.

10. Education of design engineers and managers in the use of LSI has been insufficient to date. In the final analysis, the design engineer must understand LSI in order to insert LSI into systems.

According to points 1 through 10 above, a mixture of technological and economic issues, organizational, programmatic and educational issues, and standardization emerge as principal causes of the limited use of LSI in military systems.

VLSI TECHNOLOGY INSERTION IS NECESSARY

Despite the current problems, VLSI appears to be an inevitable requirement for future systems. On-going mission analysis work and sensor system definition studies within Hughes continuously point toward more demanding signal processing tasks as illustrated in Figure 1. The technology drivers are through-put (Million operations per second, MOPS) and memory, (megabits, MBITS).

This map of existing and planned DoD/Hughes systems shows that in the near term, LSI is sufficient for meeting the performance requirements of pulsed doppler radars such as F-18, advanced tactical FLIRS (ATAC) and other sensor systems which require less than 100 MOPS and less than 10 MBITS memory.

In the early 1980 time frame, more advanced sensor systems are being planned for operational use. These systems will require the next generation of technology such as VHSIC in order to meet mission requirements.

This trend of ever increasing information gathering and processing need is expected to continue into the next decade and must therefore be planned for today in the form of new technology development programs that are synchronized with the system development program.

In parallel, a technology insertion plan must be developed by DoD and its contractors in order to provide an orderly and effective transition to the new technology.

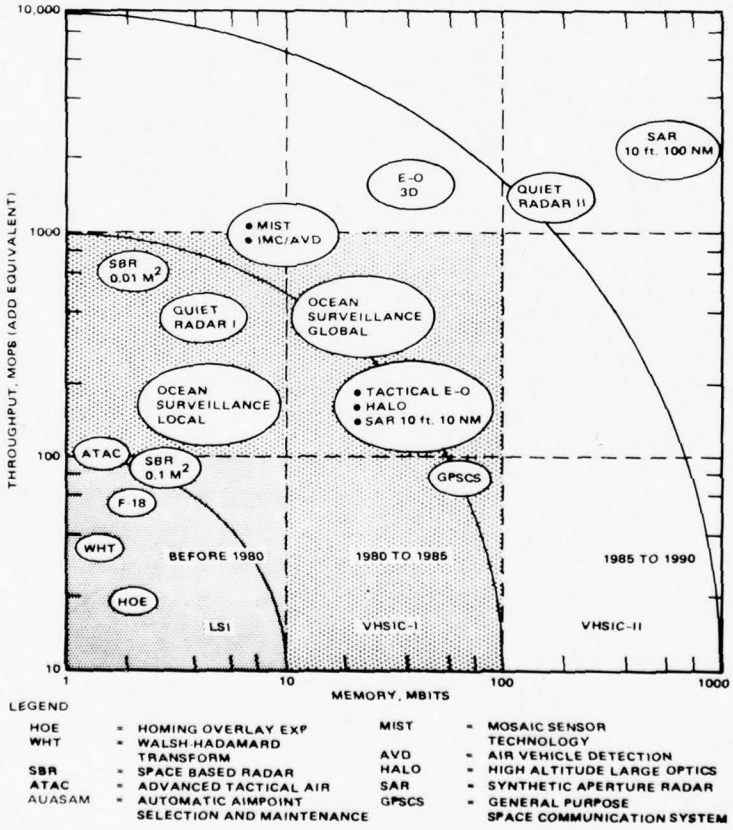


Figure 1. Sensor Processing Speed and Memory Requirements

VLSI TECHNOLOGY INSERTION CONSIDERATIONS

The decision to introduce new technology into a system must be based on one or more of the following factors:

a. Performance Improvement

b. Reliability Improvement

c. Life cycle cost reduction.

LSI, VLSI and VHSIC technology will offer weight and volume improvement in most applications. It will further provide enhanced system capability. Clearly, to be useful it must be at least as reliable as an equivalent system implemented in conventional MSI logic. Furthermore, the cost of these devices must be competitive on a per function basis with other implementations. This is particularly true in missile processors where volume and cost are major drivers. Also risk to existing systems must be minimized in order for insertion to be attractive.

Typically, complex military electronic systems do not reach full production until 4 to 6 years after the start of the design process. This time lapse allows for completion of the design, construction of engineering model hardware, engineering test program, and production line set-up. As a result, technology is already 6 years behind the current state of the art before the first unit reaches the field. By the completion of a 4 year production run, 10 year old technology is in the field. Therefore if new technology can be safely introduced at any point in this cycle then the capability of field equipment can be significantly affected.

PERFORMANCE IMPROVEMENT WITH VLSI TECHNOLOGY IN NEW SYSTEM DESIGNS

Because of the problems involved in utilizing VLSI previously discussed, committing this technology to new system designs can be very difficult. However the pay off can also be correspondingly large. The Hughes TPQ 36/37 weapon locating radars (3) provide an example of this. Advanced LSI configurations with existing functional capability may reduce the parts count to less than 10% and power dissipation to less than 20% of the corresponding current values.

The reliability of the processor subsystem, measured in terms of mean time between failure (MTBF), may increase by a factor of ten because of the reduced parts count and complexity. An LSI implementation also opens the possibility of transferring the digital processor in the TPQ 36/37 from the operations control center into the antenna-transceiver unit so that one operations control center can service several antenna-transceiver units. This is illustrated in Figure 2. The payoff to the Army in this example is reduced staffing and hence cost.

Detailed implementation comparison of the 1976 baseline Firefinder (TPQ 36/36) signal processor and the postulated 1984 VLSI version of the same processor is shown in Table 2. The existing baseline signal processor has a clock rate of 5 MHz, 39 IC/printed circuit board, average power of 159 mW/IC and a gate density of 11.1 equivalent gates/cm^2. The density x speed figure of merit (FOM) is 5.6×10^7 gates Hz/cm^2 at the module (PCB) level and 1.1×10^9 gates Hz/cm^2 at the silicon level. The factor of 20:1 reduction of FOM on the board level relative to the silicon level is due to pinouts and connector limitation. This reduction ratio may increase to 40:1 because of larger pinout requirements for VLSI.

The principal improvements that can be expected for the 1984 VLSI machine are:

1. Increased clock rate (5:1),

2. Reduced power per gate and

3. Gate density improvement of 50:1.

This translates into an improved FOM and fewer modules and module types (12 each) with an average gate density of 16,500 per IC. Total machine complexity is reduced to 36 IC with a total power dissipation of 120 Watts.

This specific design example shows the performance improvement that can be realized with VLSI in the TPQ 36/37 Firefinder system assuming that pinout limitations can be overcome with new packaging schemes such as flip-chips. In addition, higher reliability and reduced maintenance cost is expected with reduced parts count.

Other examples of this type of LSI technology insertion are shown in Table 3. The payoff in terms of logistics, performance and envelope size, weight and power is shown for EW, radar, communications and other systems. Battery cost savings may be substantial for man-portable equipment such as manpack radio. Increased mission life and utility may be significant if low power MOS/LSI were to be used in mines in place of T^2L MSI.

DESIGNING FOR TECHNOLOGY INSERTION

It is necessary to consider the problems of technology insertion during the design of the equipment and to make compatibility with technology insertion a design constraint. During the design phase it is often possible to identify near term device developments that are not sufficiently proven for the initial design but that can be inserted at a later stage. Straightforward examples of this process can be found in memory design where extra address capability is provided, allowing for system storage growth. Table 4 is a list of such examples:

1) Hughes designed the AN/AWG-9 fire control system for the F-14 in the late 60's. At that time the small radar range processor memory was complemented with four modules. However, because of the rapid rate of development of memory technology a design constraint was imposed that a single card having four times the density could be installed in any of the four card positions, quadrupling the memory size. Within two years, devices were available that allowed the 4 X density. Because no changes, other than the cards, were required in the AN/AWG-9 system, the new technology was rapidly

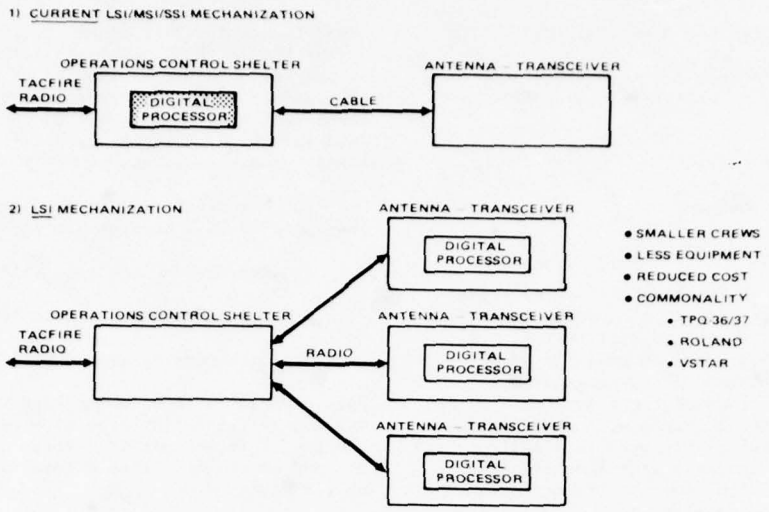


Figure 2. LSI Will Reduce Firefinder (TPQ 36/37) Equipment, Personnel and Cost

Table 2. Implementation Comparison, Firefinder Signal Processor

Parameter	1976 Baseline	1984 VLSI
Clock Rate	5 MHz	25 MHz
PC Board Size	5 x 6 = 30 in^2 = 187 cm^2/PCB	1.7 x 3.0 ≈ 5.1 in^2
Power	6.2 W/PCB	20W → 10W*
Density	39.0 IC/PCB	3 IC/Module
Power/IC	159 mW/IC	6.6 W/IC → 3.3 W/IC*
Equivalent Gates/IC	53 EG/IC	11,000 EG/IC → 5,500*
Power per Gate	3 mW/EG	600 μW/EG
Equivalent Gates per PCB	2067 EG/PCB	32,905 EG/module → 16,500*
Equivalent Gate Density	68.9 EG/in^2 11.1 EG/cm^2	6452 EG/in^2 → 3226* 1000 EG/cm^2 → 500*
Figure of Merit (F.O.M.)	20:1 { 5.55×10^7 Gate-Hz/cm^2 at module; 1.11×10^9 at silicon	{ 2.5×10^{10} at module → 1.25×10^{10}* 40:1; 5×10^{11} at silicon
Part Types	96 PCB of 58 types	12 modules of 12 types
Total Gates	3744 IC at 53 EG = 198,432	36 IC at 5,500 EG = 198,000
Total Power	596.7W	120W

Legend:

PCB = Printed Circuit Board
IC = Integrated Circuit
EG = Equivalent Gate
W = Watt Power Dissipation
FOM = Figure of Merit

*Extrapolated parameters arbitrarily reduced 2:1 to make packaging requirements more plausible

Improvement Factor (FOM) 4.5×10^2

Area x density x speed
5 x 18 x 5

EG/IC ∿ ↑ 90:1 increase
Power/EG ↓ 5:1 reduction

Table 3. LSI Benefits to Army Ground Systems

	Logistics			Envelope Size, Weight Power	Performance	
	Batteries	Sparing	De-Crewing		Density Speed	Multi-Mission Capability
EW						
Expendable JR	X	X		X	X	X
RPV JR	X	X		X	X	X
PS/MSP		X		X	X	X
RADAR						
TPQ 36/37		X	X	MINOR		
RoLand		X		X		X
VSTAR		X		X		
COMMUNICATION						
PLRS / JTIDS / ADDS	X	X		X		
Manpack						
PRC IXX	X	X		X	X	
OTHER						
Mines	X	X		X	X	X

JR = Jammer
JR/C = Jammer/Collector
PS = Platform Survivable
MSP = Multi-Sensor Platform

X = LSI/VLSI Benefits
X = Major Benefit

Table 4. Examples of Design for Memory Technology Insertion

System	Basic Design	Technology Insertion Feature	Accomplished Technology Insertion
F-14 AN/AWG 9 Range Processor	4 RAM Cards on bus	Bus allowed large capacity RAM cards	Developed large capacity single card memory replacing 4 cards
F-15 APG-63 Radar Data Processor	6 Memory Cards of 4K words each	Six extra slots plus compatibility with double density memory chips + extended addressing	12 memory cards of 8K words each
Trident Digital Control Computer (TDCC)	1 memory tray of 64K words	Three extra tray positions plus extended addressing	1 memory tray of 64K words plus 1 memory tray of 256K words

approved for insertion, saving several thousands of dollars per system and providing enhanced capability.

2) Hughes recently completed the modification of the F-15 APG-63 radar data processor memory, changing the magnetic core to semiconductor memory using 4096 bit MNOS chips. Major design changes to the radar data processor wiring and enclosures were made and new modules were developed. These changes expanded the memory from 16K words to 24K words. At the time of the design, the semiconductor vendor was developing 8192 bit memory chips. Hughes designed a memory card that would accommodate either the 4096 or 8192 bit devices and in addition provide twice as many card slots so that the memory could be doubled again. After one year of production of the 24K word memory, it is now planned to phase in the 96K word memory using 8912 bit chips and extra card slots.

3) The Hughes Trident Digital Control Computer (TDCC) is built using Standard Electronic Modules (SEM). The design allowed for expansion of its 64K word memory by incorporating extra addressing bits in the basic design. The availability of 4K static RAMS allowed a SEM module with 4 times the original capacity to be developed. With this module a 256K word memory can now be used in the existing TDCC's.

Memory technology therefore provides both examples of technology insertion and of "design for technology insertion." Because of its orderly and repetitive structure, memory has typically led the way into new technology. The challenge is to find ways to apply the same ideas to technology insertion in other areas, such as processors, input-output systems, sensors, etc.

In summary, the insertion of advanced technology into signal processors may take place during the initial design of the equipment if the new technology is sufficiently mature at that time. However, because of the rapid rate of progress of component technology, and of the high constant long life of military equipment, it will often be desirable to insert advanced technology into existing equipment that is either in on-going production or is in the field, or both.

It is therefore necessary to make compatibility with new technology insertion an initial design requirement. Some of the techniques used to allow for advanced technology are:

1. Extra memory address capability
2. Additional control bits in instructions
3. Asynchronous memory and I/O bus interfaces
4. Spare card slots, spare card pins, spare component space on cards
5. Provisions for growth in power and cooling and additional power forms
6. Hierarchical memory structure
7. "Technology transparent" designs in the sense that the system engineer interconnects functions and the technologist designs the pre-diffused wafers or the macrocells.

In all cases, the design system and the advanced technology should have the following capabilities:

1. The design systems must be in-line, and proven so that if changes are required, they can be obtained in a reasonable time.
2. "Haywire" capability, that is, the capability to modify the configuration of the system should be provided to the greatest extent possible;
3. The wafers should be produced on an existing on-going production line;
4. An authentic second source must be available and in production.

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VHSIC THRUSTS AT APPLICATIONS LEVEL

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1.0 INTRODUCTION

The Very High Speed Integrated Circuits (VHSIC) program is a major new initiative by the Department of Defense (DoD) to develop and apply integrated circuits with significantly advanced, presently unavailable, high speed, high throughput signal and data processing capability in support of military systems requirements in the 1980's and beyond.

The program is oriented principally toward applications of VHSIC to high priority Army, Air Force and Navy systems considered to be drivers of VHSIC technology. These systems will require extensive applications of very high speed integrated circuits (ICs), for signal processing functions significantly exceeding present and expected evolutionary IC capabilities, to satisfy their eventual implementation goals.

The VHSIC program differs from the broad commercial thrust in VLSI circuits in that VHSIC emphasizes development and use of ICs to provide new capabilities for broad classes of military systems for which no comparable commercial or industrial need exists. Major emphasis will be placed on achieving increased system throughputs and capacities which will require applications of previously unattainable real time signal processing implementations. Emphasis will also be placed on achieving new architectural concepts to minimize the need for design customization and thereby reduce design, logistics, and overall life cycle costs.

While the VHSIC program addresses the design of overall system concepts, it focusses primarily on the development of critical high speed signal processing subsystems which would otherwise be extremely difficult, impractical, or impossible to implement. VHSIC also addresses high speed data processing and includes the appropriate software and hardware interfaces needed to achieve a complete system capability. VHSIC cannot be expected to provide a miracle solution for all systems needing substantial decreases in cost, size, weight, and power with increased reliability. Its impact on a given system will depend on required processor speed, cost, size, weight, and power of the portion of the system applicable to VHSIC.

Overall program and technology aspects of VHSIC have been previously described in detail[1]. This paper introduces one of the four principal Army system drivers for VHSIC, CORADCOM's candidate Battlefield Information Distribution System technology, which will be considered in detail.

2.0 VHSIC APPLICATIONS RATIONALE

The four specific Army systems of interest were carefully determined based on the results of a workshop[2] to review current LSI and planned VLSI technology applications, to define areas in which VHSIC will be required to implement certain systems, and to define other areas in which substantial performance improvements can be achieved either by design into systems under development or by technology insertion. The VHSIC drivers considered were subsystems where previously unattainable mission performance could be achieved through increases of at least an order of magnitude in processor speeds and reliability, and the decrease of at least an order of magnitude in cost, size, weight, and power consumption. Systems identified as drivers for VHSIC will actually depend on the development of VHSIC to enable their implementation.

How does one decide what functions are applicable to VHSIC implementation? In areas where either functions were not realizable or where analog signal processors or multiple parallel configurations of digital signal processors were previously realizable, it is expected that implementations of new digital techniques will become practical by virtue of VHSIC's greatly increased processing speed capabilities and achievable functional densities.

VHSICs will be silicon ICs with greatly increased clock speed and programmability, as well as increased capacity to perform the functions equivalent to 10 to 100 of today's ICs. Although many signal and data processing functions now performed by combinations of multiple parallel IC configurations could be and are planned to be implemented by one or more VHSICs, the VHSIC program is not principally intended just to shrink functions of many ICs onto a single IC. Entire VHSIC chips will cost more, be larger (400 x 400 mils), and draw more power than todays ICs, but the cost, size, weight, and power per IC function will be significantly less.

The VHSIC program is essentially a systems oriented IC development program with specific plans to implement critical signal processing subsystems of selected high priority DoD systems. In view of the great potential impact VHSIC will have on the system drivers, VHSIC subsystem implementations are being considered as integral parts of the overall system programs as are the systems themselves being considered as integral parts of the VHSIC program. Plans are being incorporated into each of the overall system programs in the form of specific developments using VHSICs in testbeds for evaluation of VHSIC capabilities.

The four Army systems, together with eight systems each from the Air Force and Navy comprise the twenty DoD systems being considered in the overall VHSIC program[3].

Actual subsystem construction and system demonstrations, essential to expedite introduction of timely and affordable VHSICs into military systems, will be selected based on their potential for widespread applicability to perform military functions and missions previously precluded by computational limitations, size, weight, power, and reliability, and to reduce life cycle costs of military electronic equipment.

In order to demonstrate how systems will be addressed in the VHSIC program, one of the candidates, CORADCOM's Battlefield Information Distribution (BID)

System Technology program will be considered in detail as an example to indicate specifically the impact that the VHSIC program is expected to have on systems. Descriptions given for the various system drivers are intentionally general in the form of technical guidelines to encourage as much innovation and originality as possible for new system development during the initial program definition phase. The purposes of this initial phase are to determine the limits of feasibility and to perform analyses and develop approaches leading to implementation of VHSIC subsystems within four years according to 1.25 micrometer feature sizes and within six years according to 0.5 micrometer feature sizes. The latter implementation is expected to provide a capability for further major improvements in system performance by projecting subsystem design concepts to higher performance levels and by extending the state-of-the-art to include submicrometer feature sizes and associated higher circuit densities.

3.0 BATTLEFIELD INFORMATION DISTRIBUTION TECHNOLOGY

3.1 Description and Requirements. Deficiencies of conventional Army communications have become apparent during the past few years in areas relating to real time data communications and ECCM. Recognition of these deficiencies, and the positive need to provide data distribution capabilities for the mobile transmission of information in digital form covering thousands of users over a wide area from FEBA to Corps Rear, have led to the quest for new approaches to tactical data communications for the 1980's. Examples of typical battlefield users requiring these new capabilities are shown in figure 1. CORADCOM has been specifically addressing these deficiencies and needs in information distribution since 1975 and is currently conducting high priority Battlefield Information Distribution (BID) technology program to develop new radio based data communication concepts. BID is a generic name given to the class of technologies which will support development of a ground based, mobile, real time, jam resistant information distribution system for the 1990's.

The need exists to efficiently distribute real time digital information for tactical automated systems involved in acquisition and processing of target data and control of weapon systems, provide interoperability among automated data systems, while providing low bit rate voice and relative navigation capability. This new BID technology must support continuity of operations, so that information can continue to flow even as elements of the system are destroyed or fail, and must be fully secure and adequately jam-resistant.

The Army is in the process of developing and fielding a new generation of systems which provide for the delivery and control of the majority of fires delivered on the battlefield. These systems identified thus far which require reliable real time data exchange include air defense (Air Defense Command and Control System AN/TSQ-73), combat electronic warfare and intelligence (Technical Control and Analysis System), command and control (Tactical Operations System), and fire support (Tactical Fire Direction System).

The communications system utilized by these automated systems must:

(1) provide high capacity, real-time, jam-resistant, digital data exchange to service a large number of users.

(2) have sufficient flexibility to support the Command, Control and Communications (C3) structures and provide for compatible interfaces among diverse Army systems requiring real-time information distribution.

(3) exhibit a low probability of intercept (LPI) characteristic.

(4) have self-contained COMSEC so that cooperating terminals can communicate with each other in a secure, netted mode of operation for real time information distribution.

(5) provide integral ECCM capabilities sufficient to defeat the threat.

(6) provide integral position location capability.

The basic concept of BID is designed to build the technology base to support the eventual development and fielding of a system in the 1990's. While an interim measure using Position Location Reporting System and Joint Tactical Information Distribution System elements (PLRS/JTIDS Hybrid) is currently being investigated to provide initial operational capability in 1985, the Army is also addressing longer term solutions to provide real time battlefield information distribution using other technologies with capabilities such as those provided by the Packet Radio System. Although technology projections indicate that BID objectives are expected to be partially accomplished using projected state-of-the-art technology, significant technical barriers related to implementation at increased signal processing speeds and decreased cost, size, weight, and power remain to be overcome to permit extensive deployment of such a system. In order to determine what portions of BID are applicable to VHSIC implementation, the following guidelines are provided. The block diagram of a generic BID system is shown in figure 2. Whether the eventual BID consists of Packet Radio, PLRS, JTIDS, or some yet to be determined "Brand X", which might be either totally new or combinations of the above technologies, the basic building blocks of a system needed to perform the already identified wideband spread spectrum data communications are well known. In the implementation of BID, the areas in which it is felt that VHSIC will have the most significant technical impact are in system capacity, anti-jamming capability, and network management.

3.2 System Capacity. Although signal processing theory has been extensively developed, the technology needed to support real time signal and data processing and information distribution has not advanced to the point where cost effective implementation is realizable at the increasingly higher data rates and throughputs required. In order to increase system capacity, significant increases in circuit speeds are needed to process and determine the eventual disposition of a received message.

3.2.1 Multinetting. Methods of increasing overall communication system capacity may include multiple simultaneous use of a network in sufficiently separated geographical areas, or establishment and use of multiple independent networks within the same geographic area.

The propagation mechanism of a BID network is essentially line-of-sight, with some multipath, aided by retransmission through flexible, non-dedicated relays. Simultaneous transmission of messages among network users not within line-of-sight of each other effectively increases a given network capacity.

Multinetting is the process whereby independent communications can take place simultaneously among different combinations of network subscribers in the same area. Techniques for achieving such capabilities involve operating each net on a different frequency or using code division multiple access techniques where each network uses different spread spectrum codes in the same frequency band. An example of multinetting where field artillery and air defense users could be placed on different functional subnetworks is shown in figure 3.

In order to accomplish multinetting, each subscriber radio must be able to receive and transmit on more than one network. Ideally, the capability to receive messages on several networks simultaneously, as opposed to scanning networks to receive only one message at a time, should be provided. Such advanced capability will require multiple Radio Frequency (RF) front ends and/or multiple spread spectrum code generators and correlators.

The high speed processing capability needed to support multinetting is substantial. The capability to receive and process messages simultaneously roughly multiplies the amount of signal and data processing circuitry required for one network by the number of networks for which simultaneous operation is needed. Even if reception on only one of several networks is necessary at a given time, the amount of signal processing circuitry for data synchronization and detection multiplies that portion of the circuitry by the number of networks for which simultaneous detection is needed. The benefit of VHSIC in either case is that, instead of needing several complete radios operating on different networks, only one radio containing multiple sets of high speed signal processors is needed for simultaneous detection and reception.

3.2.2 Low Bit Rate Voice. In the area of digitized voice there is continuing interest in reducing bit rates as low as is feasible while retaining acceptable quality for communication. Current technology has reduced 16 kilobits per second continuously variable slope delta (CVSD) modulated voice to a commercially available chip. At lower rates on the order of two kilobits per second, other techniques such as linear predictive coding (LPC) appear to be very promising to provide a voice capability for BID users while maintaining high capacity primarily for users requiring data transmission. These newer techniques have been restricted until recently to a laboratory implementation environment, because of their associated processing speed, equipment complexity, cost, power, size, and weight.

It is not known which technique will eventually be used to implement low bit rate voice for BID, but it is likely that the high speed processing circuits applicable to any technique will be worthy candidates for VHSIC.

3.3 Anti-jamming Capability.

3.3.1 Modems. In order for VHSIC chips to have their broadest possible future applicability, and thereby be more cost effective, they must possess capabilities for a reasonably wide variety of functions. A prime example of this is in the area of spread spectrum modulators/demodulators (modems) to provide anti-jamming capability. In addition to having broad applicability throughout DoD for future standardization of modem components, VHSIC signal processing capabilities will enable designs such that all communication links can be provided with significant amounts of anti-jamming protection, and the

availability of VHSIC modem components will eliminate the need for costly duplicative design efforts. There are many functions which are generally applicable to all modems, but in order to achieve the broad applicability desired, design emphasis for VHSIC must be placed on programmability for those functions and parameters which must remain system specific. It should be possible in VHSIC to analyze DOD's modem requirements to determine the common functions and the specific ranges of capabilities needed in modulation schemes, data rates, and operational protocols. The common functions could then be made available on chips in conjunction with programmable capabilities for a multiplicity of modulation schemes, rates, and protocols. Modulation schemes such as AM, FM, SSB, FSK, PSK with variable rates and combinations of pseudo noise coding and frequency hopping would be possible with additional programmability provided for software protocols.

3.3.2 Matched Filters and Frequency Synthesizers. The reception of spread spectrum signals requires the correlation of incoming data with a known spread spectrum code in a matched filtering process. Available state-of-the-art devices currently used for matched filtering are primarily surface acoustic wave (SAW) devices and charged coupled devices (CCD). While the digital matched filter is theoretically a strong candidate for this application, its implementation at the speeds necessary for BID is not currently available due to limitations in hardware capabilities associated with high speed signal processing, cost, power, and complexity. Since each spread spectrum code requires a different matched filter, it initially appears that attempts to achieve commonality and widespread applicability are unlikely. With processing speed and programmability features to be inherent in VHSIC, however, it appears that development of a universal programmable matched filter may be feasible for many applications within yet to be determined code length and speed limits. The programmability capability will be needed to correlate rapidly changing code patterns on a bit-by-bit basis to provide anti-jamming protection, while providing for multiple waveforms, and multiple receivers to improve anti-jamming performance.

For example, in the generation of spread spectrum modulation for requirements such as BID the techniques under investigation include direct sequence pseudo noise, frequency hopping, or combinations of both. It is expected to be possible to provide ranges in the number of chips per bit for pseudo noise code generation and ranges in the rates and patterns of frequency hopping. Capabilities for pseudo noise coding at rates of 100 million chips (100 megachips) per second and more are needed to provide anti-jamming protection greatly exceeding that currently available.

Frequency synthesizers needed to support spread spectrum for BID pose particularly stringent requirements in power consumption and size requirements for frequency hopping and direct sequence pseudo noise as well as in high speed switching and settling time to support frequency hopping. Depending on actual implementation, the use of multiple synthesizers may be needed to support both multinetting for capacity increases and multiple receivers for anti-jamming protection. For synthesizers, VHSIC appears to be particularly applicable to implementing high speed digital frequency division circuitry for either spread spectrum modulation technique. Where the high speed processing to generate and correlate extremely wideband direct sequence spread spectrum codes will require VHSIC, high speed switching for frequency hopping will require VHSIC but the matched filter correlation function for narrowband codes used in frequency hopping probably will not require VHSIC.

For widespread applicability and commonality, however, it may be beneficial to combine high speed programmable matched filtering and synthesis circuitry in VHSIC to support both spread spectrum techniques. Examples of VHSIC applications in this area are shown in Figure 4.

3.3.3 Error Control Coding. While basic modems have become commonplace and diverse, and spread spectrum modulation has continued to develop and be applied, applications of error control coding appear to be yet in their relative infancy. Error control coding is an example of a technique required for BID whose theory was extensively developed during the 1950's and 1960's but whose practical implementations were limited through the 1960's to relatively simple techniques. The advent of LSI in the early 1970's made it feasible to implement moderate length and speed block and convolutional codes. The implementable designs were both practical and useful in improver error rate performance, thereby increasing data reliability in noise and jamming environments. While LSI versions were generally designed for particular codes, the use of VHSIC is expected to enable practical implementation of a subset of the more useful coding techniques currently known in one or two programmable ICs with appropriate interface options.

3.4 Network Management. Although signal processing is the main thrust of VHSIC applications, there are also significant needs to support use of VHSIC for increasingly higher speed data and message processing. A very important example of such an application is in the real time network management of large data networks such as a BID Network.

Network Management is essentially the execution in real time of a set of rules and procedures, implemented in computer decision logic, which controls the movement of information as well as the overall behavior of a network. Previous techniques used centralized network management wherein a single radio network node contained sufficient hardware and software to perform all required network management functions. The main problem with such a centralized technique is that a single network participant managing a network is highly vulnerable to destruction or jamming, rendering the entire network unusable. In the BID Technology program, distributed automated adaptive network management techniques are being investigated to support fully automatic mobile operation in a dynamically changing battlefield environment. The types of functions which must be performed include initialization, network control, channel access control, flow control, congestion control, relay management, routing (both assigned and dynamic alternate), stability control, routine monitoring of operational status and traffic statistics, and the control of information flow through gateways to other networks. In the implementation of a BID network, there is substantial interest in applications of VHSIC in the area of information processing to implement processor control functions and provide distributed network management capabilities as far as is feasible, practical and cost effective.

3.4.1 Distributed Network Management. Trends toward distributed processing capability are evident in the evolution of large centralized computers of the 1950's and early 1960's to minicomputers in the late 1960's to distributed microprocessors of the 1970's.

The concept of distributed network management will make use of the continued evolutionary development in computer processing, but the speed, power consumption, cost, size and weight of available microprocessors, memories and

associated hardware cannot currently support such a concept.

In addition to increasing capacity and providing more efficient network operation, the most important benefits to be gained are associated with improved survivability in a tactical environment through automatic self reorganization of network resources remaining after failure or destruction of other network elements. Factors to consider in the implementation of network management include the size of a network and its capacity in terms of users and/or data rates, characteristics of users in terms of whether messages are random or periodic, relatively short or long, the degree to which network management is distributed, and the number of simultaneously operational networks which must be internetted.

The example given for multinetting concepts in Figure 3 also shows several subnetworks sharing traffic loads and control functions for the covered area, and demonstrates a trend toward distributed network management. The implementation of distributed network management will require the currently unfeasible real time execution of large numbers of computationally complex algorithms in each network subscriber radio, and the capability for millions of words of memory for storage of programs and network status information. VHSIC triggered advances in the state-of-the-art will permit distributed network management to an extent not before possible, and therefore, will make possible all of the benefits such as survivability, efficiency, and automatic control capability.

Techniques currently in use in systems to achieve greater processing speeds make use of two or more microprocessors, functioning and sharing a data bus simultaneously in a multiprocessing mode, complementarily accomplishing portions of the total processing requirements. The need for multiprocessing is driven primarily by requirements for microprocessors to execute instructions at rates which exceed their capabilities.

In addition, the use of two microprocessors doesn't provide twice as much processing capability or throughput, while more than twice as much power is consumed. The inefficiency of this technique stems from the requirement for additional hardware and software for interfacing and sharing data bus control.

Microprocessors expected to be developed in VHSIC will provide greatly increased rates which will reduce the need for multiprocessor implementations. This is not to say, however, that multiprocessing should be eliminated from future consideration as computational requirements for signal and data processing are likely to continue to increase, The application of parallel pipeline processor architectures are also expected to play an important role in VHSIC development. It is the availability of VHSIC that is expected to make the implementation of fully distributed network management possible.

3.5 BID/VHSIC Program Definition. The needs described above for BID have led to the following statement of objectives for the BID portion of the VHSIC FY-80 Program Definition phase:

(1) To develop a detailed system and program development plan for implementation of brassboard prototypes of critical processing subsystems for information distribution within four years according to 1.25 micrometer feature sizes. The plan must define and scope all of the related VLSI, VHSIC

fabrication technology development efforts that must be conducted in a systematic manner, to insure successful implementation of the brassboard system development.

(2) To develop a plan for a parallel effort to provide a longer range capability for additional major improvements in system performance based on further extension of the VHSIC state-of-the-art to submicrometer feature sizes. The anticipated capability will be expected to provide significant increases in ECCM and data network capacity in a distributed network management environment with additional reductions in power consumption, cost, size, and weight.

Significant increases in ECCM and anti-jamming capability will be achieved through the use of advanced signal processing and spread spectrum modulation at rates in excess of 100 megachips per second with appropriate error control. Additional system capacity will be achieved through the use of simultaneous multinetting capabilites. Subsystem modules to provide additional capabilities to approach the overall technical objectives will also include robust single-chip low bit rate speech processing based on projected state-of-the-art, a universal programmable frequency synthesizer, and all-digital intermediate frequency (IF) signal processing at rates of approximately 200 to 300 megahertz. These additional capabilities will then be available for incorporation in other evolving communication system applications.

4.0 CONCLUSION

This paper has mainly discussed applications of VHSIC to Army communications and has shown some of the benefits to be derived in applying VHSIC to high speed signal and data processing. In considering the technology needed for increased system capacity and anti-jamming performance, it is seen that VHSIC is directly applicable to the digital portions of the spread spectrum modulator/demodulator (modem), including particularly the chip encoder, correlator and error control techniques, and is also directly applicable to digital portions of the frequency synthesizer and to low bit rate voice processing. In the interests of achieving widespread applicability of VHSIC, the overall program is concerned with many diverse system applications of the Army, Air Force, and Navy. It is expected that, since the signal processing requirements of these high priority systems are the most stringent currently envisioned for the military, some reasonable number of VHSICs may be developed for these systems which will also be widely applicable as "building blocks" for many others. In examining the signal and data processing needed for BID and other advanced digital communications systems, for example, it is likely that a subset of the eventual VHSICs could be configured to generate any one of a number of specific hardware designs with modular memory capacity, leading to development of a common multipurpose programmable communications terminal. The old cliche "it's only a software change" would in fact be true as far as the operational hardware is concerned since the VHSICs will stress programmability. For each different system application, the software required to operate the system would be significantly different and would be loaded into memories for insertion into that system.

Although VHSIC is not directly applicable to analog processes, just as some of today's ICs include hybrid analog and digital circuit implementations on the same chip, it is likely that future ICs will combine both analog and

VHSIC type digital implementations.

The work accomplished to date is only the "tip of the iceberg" so to speak in that the Army, Air Force, and Navy have jointly defined the VHSIC program and industry has started to formulate approaches to achieve VHSIC goals. The FY-80 Program Definition Phase will serve to define in detail potential technologies and application approaches to develop VHSICs for DoD systems.

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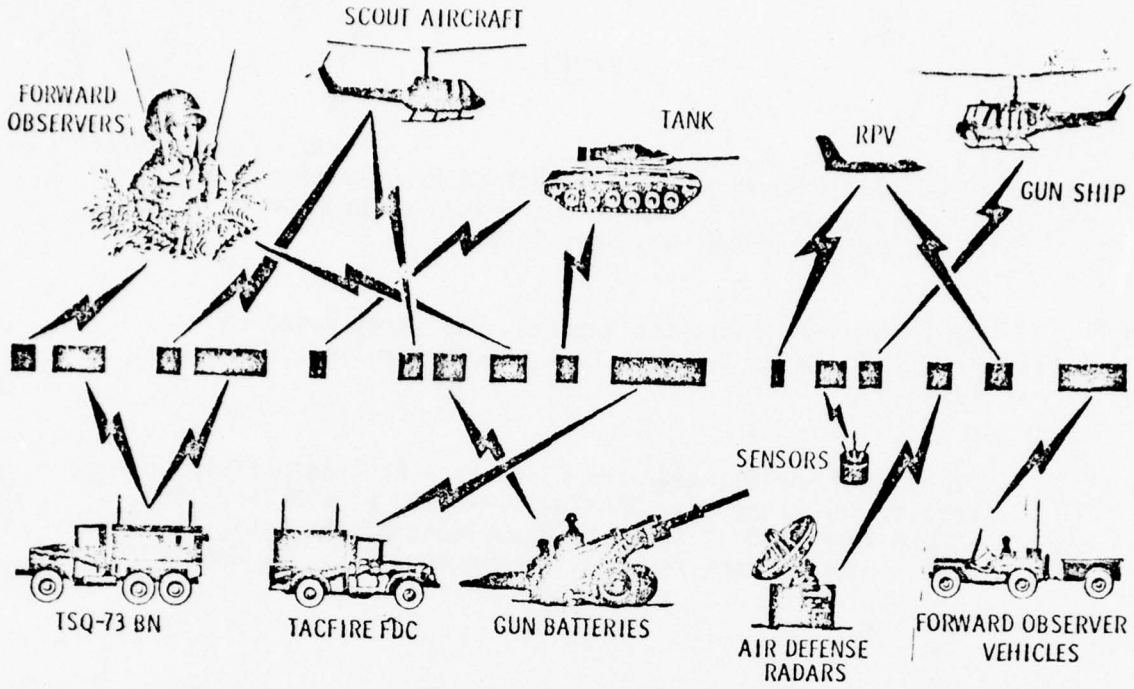

FIGURE 1. TYPICAL BATTLEFIELD DATA COMMUNICATIONS USERS

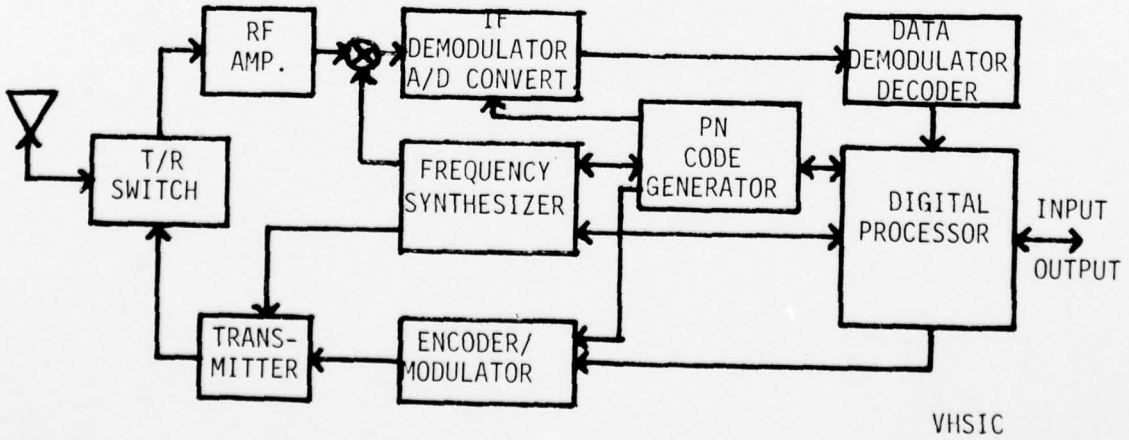

FIGURE 2. GENERIC BID SYSTEM

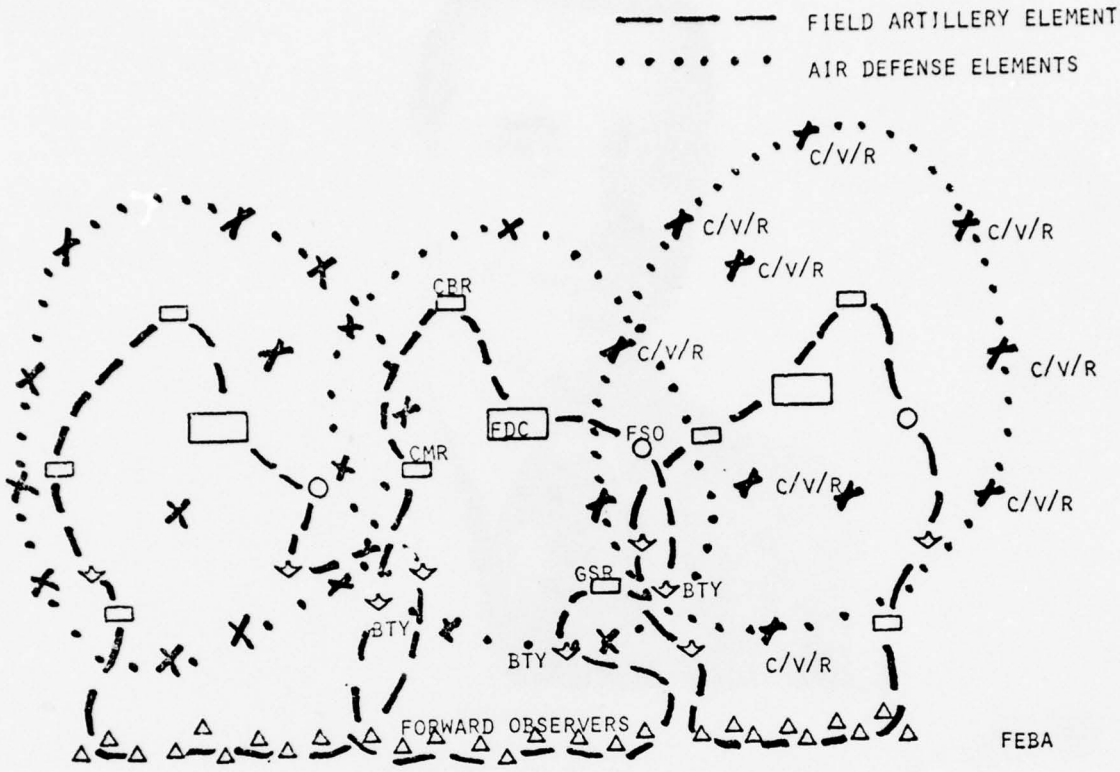

FIGURE 3. MULTINETTING/DISTRIBUTED NETWORK MANAGEMENT

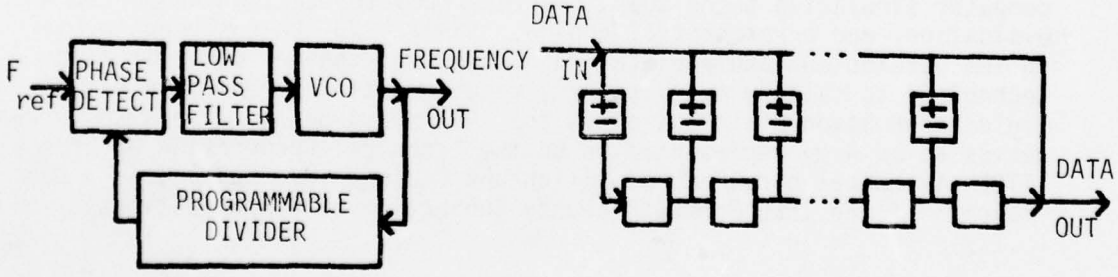

FIGURE 4. FREQUENCY SYNTHESIZER AND MATCHED FILTER

BIOGRAPHY

JOHN EUGENE QUIGLEY

Mr. Quigley was born in Red Bank, New Jersey, on 8 April 1942. He received the Bachelor of Engineering degree from Stevens Institute of Technology in 1963 and the M.S.E.E. degree from Newark College of Engineering in 1969.

In 1963, Mr. Quigley joined what is now the Communications Systems Center of the U.S. Army Communications Research and Development Command. Between 1963 and 1974, he participated in various efforts to advance HF, VHF, satellite, and troposcatter communications through applications of computer simulation techniques, channel characterization and performance evaluation, and error control coding. Since 1975, he has been involved in the development and application of state-of-the-art communications technology to satisfy evolving Army requirements for real-time battlefield information distribution in the 1980's and beyond. He also currently serves as an Army representative on the Technical Cooperation Program (TTCP) technical panel on Modulation and Coding. Mr. Quigley is a past chairman of the IEEE Monmouth County Subsection on Communications.

TECHNOLOGY INSERTION CONCEPTS FOR THE MILITARY COMPUTER FAMILY

by DR. EDWARD LIEBLEIN

US ARMY COMMUNICATIONS RESEARCH AND DEVELOPMENT COMMAND

ARMY BATTLEFIELD AUTOMATION PROBLEMS

The increasing complexity, speed, and lethality of modern warfare has made automation on the battlefield essential for weapon system and equipment control and to provide the commander with an up-to-the-minute grasp of battlefield facts from which he can make decisions. The introduction of computers, software, peripheral devices, and terminals into such systems has been accompanied by a series of problems: (1) proliferation, (2) sole-source acquisitions, (3) old hardware, (4) software lock-in to old hardware, (5) intersystem incompatibility, (6) potential loss of continuity of operation, (7) excessive life-cycle costs, (8) difficult evolution to accommodate changing requirements, (9) increased time for development and fielding, and (10) operational software errors.

Today, there are 30 different computers used in the 27 automated Army tactical systems now either in production or deployed. A survey of 49 Army systems currently in development indicated the planned use of 35 different computers. A survey of 128 systems revealed the selection of fifty-seven different computers for 92 of these systems.

Computers are at the tip of the proliferation iceberg. Hidden beneath the surface is a wide range of languages, software development and support systems and related software tools, instruction-set architectures, and terminals and peripheral devices. The need for some form of standardization is obvious, but any effort along this line must also heed the call for competition in computer acquisitions and the call to make maximum use of industrial developments and off-the-shelf products. This apparent "catch-22" situation must be resolved.

As with any standardization program, there exists the risk that we will find our systems using obsolescent hardware during a major part of the deployment period. The issue with respect to obsolescent hardware involves more than our simply wanting the best hardware for our forces. It involves our potential inability to provide effective maintenance. The bottom line may be the existence of weapons/C^3I systems in the field that are difficult to keep running and whose performance is inferior relative to those of a potential enemy. The problem may be particularly severe with respect to systems that use computer products since advances in this area have been quite rapid. Speed and density have been doubling approximately every three years, power and weight continue to be reduced, and reliability continues to improve.

The dilemma arises because computer technology is expected to advance by about an order of magnitude between the time of conception and the time of fielding of a computer-based system.

Even if hardware upgrade could be accomplished in a timely manner with respect to either systems in development or to systems that are already fielded, there is another potentially serious problem lurking, namely that of lock-in of software to specific computers and their instruction sets. Should widespread hardware, language, and instruction-set architecture proliferation continue, it will be impractical to upgrade technology without redoing software at the same time, which could be extremely expensive. Thus, if we continue on our present course we will lock more and more of our software into a large number of instruction-set architectures embedding into older hardware, and proliferation will remain the rule.

Under such conditions, intersystem interoperability problems (complicated by proliferation of physical interfaces, executive/software interfaces, and languages) may be severe. It is also expected that the proliferation of incompatible equipment will adversely affect the ability of an automated battlefield to survive. Current manual (non-automated) battlefield systems, although slow, have inherent flexibility and can be reconfigured dynamically owing to the interchangeability of key equipment in the major functional elements of the command post. Hardware interchangeability facilitates damage recovery and allows the commander to reconstitute his organization so that the essential functions of the entire command post can be carried out with whatever elements remain undamaged/functional. Automation, however, may increase system capacities at the expense of operational flexibility. As we move toward the automated command post which will be part of the battlefield system network of the future, it is essential that we maintain the potential for continuity of operations that exists today. The problem has been stated well by Lt. General Hillman Dickinson, Director of Command, Control and Communications, Joint Chiefs of Staff: "I cannot emphasize too much the extremely high cost of multiple logistics systems ... where the cost of a replacement part is not measured in the price to buy that part, but in aircraft sorties to deliver it in emergencies, loss of men and equipment on supply runs; overall a price that can hardly be over estimated."

GOALS OF THE MCF PROGRAM

The problems described above have been translated into a set of goals which, if met, should mitigate the difficulties of developing and deploying battlefield automation.

Acquisition Essentials

There are several goals that relate directly to the strategy pursued in the acquisition process:

a. Real competition that is sustained throughout the acquisition life cycle.

b. Technology insertion throughout the life cycle to take advantage of rapid advances in computer technology in order to realize improvements in reliability, performance, capacity cost, size, weight, and

power.

c. Overall reduction of costs over the entire life cycle of both software and hardware.

d. Overall reduction of time for both development (of hardware and software) and production (of hardware).

e. Avoidance of unnecessary proliferation of hardware, software, languages, architectures, and software support systems.

Survivability

This goal is concerned primarily with the ability to achieve continuity of operations under battlefield conditions. Factors include:

a. the reliability of hardware and software

b. maintainability (fault detection, fault isolation and parts replacement)

c. interchangeability of parts

d. degraded mode operation/graceful degradation

e. load shifting

f. operational reconfigurability

g. effectiveness of logistics support

h. effectiveness of maintenance support

System Evolution Flexibility

To date, very few battlefield automation systems have been fielded. It is anticipated therefore, that during development and after deployment initial implementations will be required to evolve as operational experience is gained and user needs become solidified. It is essential that such evolution be readily accommodated. This requires that the MCF hardware, instruction-set architecture, language, and software have the flexibility to support system functional expansion and change, and technology insertion.

AN INTEGRATED APPROACH

The overall approach being taken to meet the goals described above is to provide a wide range of capabilities (both for development and deployment) via a "family" concept. Included in the family, is a plug-compatible set of hardware products (including computers, peripherals, terminals, interfaces, configurations and installations), a set of generic software products (to be fielded), instruction set architecture (ISA) and a software development and support system (including high order language, compiler, and software tools).

It is intended that the MCF members will constitute a standard approved product line which battlefield automation program managers will be required to use. It is anticipated that MCF products will be readily available so that program managers can begin immediate system/software development.

The MCF operational/support concept involves common intersystem interfaces, the interchangeability of hardware within and across systems, the use of common software support systems, common logistics and maintenance support, reduced numbers of types supported, and technology/performance upgrade on a plug-compatible basis.

The MCF acquisition strategy involves establishment of multiple qualified suppliers of items that are specified on a form, fit, and function basis, centrally controlled procurements, off-the-shelf availability, the establishment of large production bases for use in systems Army wide, and open competition for each acquisition. In combination, the standard family concept, acquisition strategy, and operational/support concept of the MCF project are planned to address all of the problems outlined earlier.

There are many levels at which computer system standardization can be effected including high order language, instruction-set architecture, external bus, box, module, card and build-to-print levels. The MCF approach will involve standardization at several of these levels. Discussion of the specific approaches being pursued in the MCF program in software, ISA, and computers is contained in subsequent paragraphs.

SOFTWARE

The high order language of MCF will be the new DOD/Tri-Service developed language, Ada. This Pascal-based language has been optimized for use in the development of software for embedded computer systems. Elimination of the use of assembly language was an important requirement. Since real-time systems involve tightly interleaved and time interdependent processes, and coupled parallel (possibly distributed) processes, it was required that the language provide explicit capabilities for such functions. Machine independence also was established as a requirement in order to achieve transportability of software developed using Ada. Error resistant features (exception handling) that provide the ability to control events when hardware or software errors occur were required as well.

Award of a two year contract for a transportable Ada compiler is planned for the November-December 1979 time frame. The compiler will initially be hosted on the VAX-11/780 and will run under the VMS operating system. Initial code generators will be developed for the VAX, AN/GYK-12, and PDP-11/70 ISA's. Run-time support packages will be provided that will perform executive/operating system functions. It is expected that testing and certification of the compiler system will be completed by June 1982.

An advanced software tool, the Design Analyzer, will be developed for the MCF under a separate contract. The Design Analyzer, which will utilize a methodology called high-order software, is oriented toward the avoidance of errors in the system specification and software design processes. It is expected that the Design Analyzer will be available for trial use in July 1980.

Additional software tools to be developed include a Structured Design Diagrammer and software management oriented tools such as a Version Controller.

INSTRUCTION-SET ARCHITECTURE

It was originally planned that the standard family of tactical computers employ a single instruction-set architecture. Analyses conducted by the Computer Family Architecture (CFA) Committee led to the recommendation of the instruction-set architecture employed in the PDP-11 product line as the ISA for MCF. A significant consideration in this recommendation was the announced plan for a 32-bit member of this product line (later called the VAX-11/780). Early plans included the 16-bit PDP-11 ISA and its 32-bit successor ISA as mainstream ISA's for the MCF program. In an attempt to capture tactical software already developed or being developed for other ISA's, a multi-architecture approach was conceived that, if successful, would permit change of the ISA "personality" of an MCF computer by replacement of a subset of its plug-in modules, namely the CPU module, and the high speed and low speed bus interface modules. To be included within the MCF ISA context were those ISA's native to the following computers: AN/GYK-12, AN/UYK-19, AN/UYK-7, AN/UYK-20, AN/AYK-15A, AN/AYK-14, PDP-11, and VAX-11/780. As time moved on it became apparent that very high risks were involved in such an approach and that the program in an attempt to solve all of the problems might end up solving none. A less risky approach was adopted. The attempt to "back-emulate" existing ISA's was dropped, and a decision was made to employ a single ISA. Analyses and experiments that were conducted concluded that the VAX (or a VAX-like) ISA would be significantly superior in terms of memory requirements and performance to the other ISA's in the competition. (This type of ISA is specifically oriented toward high order languages, having powerful instructions that directly implement HOL constructs. Further, the 32-bit virtual address offers the potential to simplify software development and eliminate the cost of context switching overhead that usually must be paid when 16-bit address ISA's are used in systems with large memory requirements). The MCF program, then, will pursue the use of a single 32-bit ISA in lieu of implementation of a wide range of ISA's via plug-in modules. (Toward this end, the Army has been negotiating an agreement with Digital Equipment Corporation for support with respect to the VAX-11/780).

COMPUTERS

Modular computer hardware (nomenclatured AN/UYK-41) will be designed that will provide the ability to configure computer systems with a range of capacities and performance levels from a limited set of standard boxes, cable types and standard peripheral devices. To accommodate technology insertion, modular elements will be defined by form, fit, and function (F3) specifications rather than by specific detailed drawing. All equipment will be designed and built to permit sustained operation in tactical environments. Initially, four performance levels were specified, however, it is expected that this number will be reduced. Other matters also currently being readdressed in the program include level of modularity (box vs. module), need for specification of an internal backplane bus, packaging strategy (ATR cases, cabinets, large boxes, card size/type), reliability, volume, logistics and maintenance support approaches, technology insertion approach, approach to competitive acquisitions, and program schedule.

Earlier in the program, the computer system was to have been partitioned (on an F3 basis) at the levels of modules (CPU modules, memory modules, power converters, bus interface modules, bus extender modules, etc.) each of which, essentially, consisted of an integrated collection of cards. Each module type was to have been produced by at least two suppliers according to F3 specifications and such modules were expected to operate in place of each other (plug-compatibility). Analyses have questioned the feasibility of such an approach at the module level chosen for the MCF. The issue is whether F3 specifications at this level can be produced that are complete, consistent, and unambiguous. While use of F3 specifications has proven successful in the airline industry, where high level, end item functions have been specified, the risk is believed to be heightened significantly when the F3 item is not an end item but is a piece of a computer such as a bus interface module, or a CPU where such modules interface each other via a high speed internal bus. While analysis in this area is ongoing as of this writing, it is believed that a shift of F3 modularity to the box level, say to the level of an ATR case where such case would, in effect, contain an entire computer/which may then be augmented by other cases for expansion of memory and input-output capabilities) would reduce program risk significantly. In such an approach, technology insertion in the memory area could be accomplished readily, as could it with regard to the basic computer box.

Another approach to achieving technology insertion in the face of rapid advances in semiconductor computer logic and memory technology (over the last decade, chip complexity has increased approximately four orders of magnitude and the cost per gate has declined correspondingly), is to compete the computer acquisition and award a five year fixed-price requirements contract that provides for a priori established pricing levels according to quantities purchased. As technology advances the contractor would be afforded the opportunity to propose to the government the introduction of advanced lower cost technology which, if approved, could result in greater profit for the contractor and improved products for the battlefield. Another approach might be to (cyclically) compete and award a new development with associated five-year requirements contract on the heels of the existing effort (with a minimum amount of overlap) to assure the continuing introduction of new technology in a competitive environment.

The approach to achieving competition and technology insertion must consider seriously the implications with respect to logistics and maintenance support. Greater reliance will have to be placed on built-in test functions. Repair may have to be relegated to the manufacturer (possibly to depot or General Support levels) in order to effect timely fielding of original and improved products (due to the elimination of the need for the development of maintenance documentation and training courses, and the elimination of training time, including validation of the effectiveness of such training). The cost of increased reliability achieved through either the use of more expensive lower power components, lower packing densities, or through redundancy/fault-tolerance will have to be evaluated against possible corresponding savings in the cost of logistics and maintenance support, and the potential for earlier use of items with superior performance on the battlefield.

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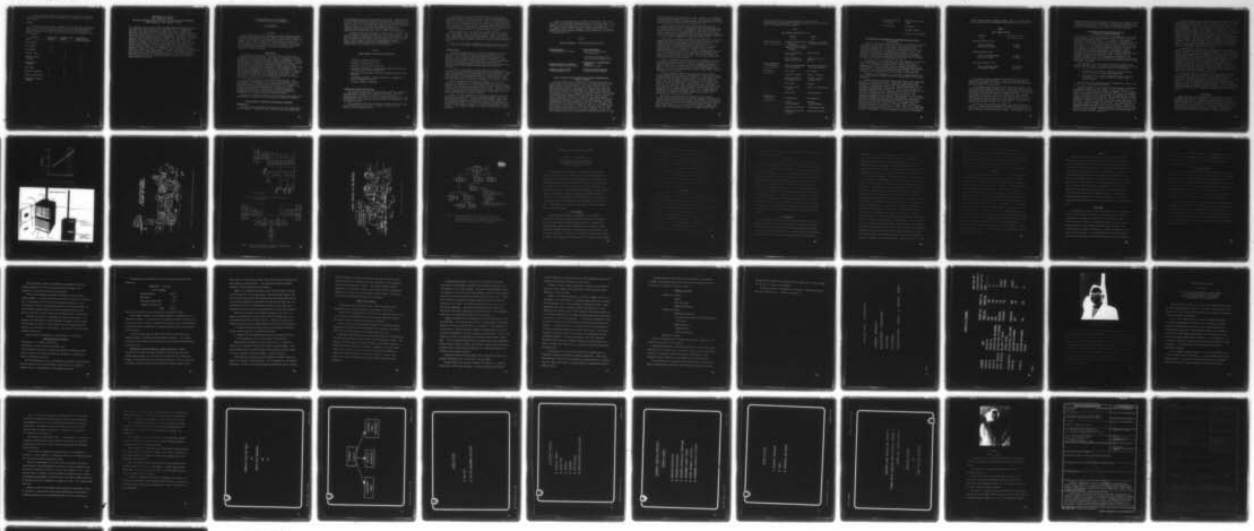

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The issues delineated above are expected to be resolved by the end of January 1980 and contract award is planned for late FY80 or early FY81 for MCF computers.

SUMMARY

The MCF acquisition strategy, standard family concept, and operational/support concept collectively must address the current and anticipated problems associated with the development and fielding of Army battlefield automation systems. The areas to be attacked by each are described in the matrix below:

APPROACH / ISSUE	ACQUISITION STRATEGY	STANDARD FAMILY CONCEPT	OPERATIONAL/ SUPPORT CONCEPT
PROLIFERATION	X	X	
SOLE-SOURCE	X		
OLD HARDWARE	X	X	
SOFTWARE LOCK-IN		X	
INTEROPERABILITY PROBLEM		X	X
SURVIVABILITY PROBLEM		X	X
HIGH COSTS	X	X	X
DIFFICULT EVOLUTION		X	X
LENGTHY ACQUISITIONS	X	X	
OPERATIONAL SOFTWARE ERRORS		X	X

BIOGRAPHICAL SKETCH
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Dr. Lieblein received the BEE and MEE from New York University in 1955 and 1963 respectively, and the Ph.D. in Computer Science from the University of Pennsylvania in 1968. He has been employed at Fort Monmouth, N.J. since 1955 where he has worked on computer system developments, computer architecture, iterative machine arrays, languages, compilers, operating systems and tactical software systems. He was Chief of the Software Engineering Division in the Center for Tactical Computer Systems from 1975 to 1978 and has been instrumental in the development of the new DoD high order language, Ada. Since November 1978, he has been Director of the Military Computer Family Project at CORADCOM. Dr. Lieblein has been affiliate associate Professor at Stevens Institute of Technology and lecturer at Monmouth College. He is currently Adjunct Associate Professor of Computer Science at the University of Pennsylvania where he teaches graduate courses in compilers and operating systems.

SOME OBSERVATIONS ON THE TRANSFER OF INFORMATION DISTRIBUTION TECHNOLOGY

D. L. Nielson
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ABSTRACT

With rapid strides in the technology of data communications great potential exists for improving the information distribution methods available to commanders, but several major problems loom to prevent this change. After a brief review of what technology has to offer, we examine three of those problems: the lack of standard data structures and interconnection, the assimilation and utilization of information, and the inherent contradiction of distributed information and hierarchical command structure.

Introduction

By everyone's admission we are in the midst of a revolution in information generation and flow. The number of information sources is consistently increasing and the means to deliver information, at least electronically, is becoming evermore available and affordable. But what of our ability to assimilate or use this information? How does one use raw information, arriving at unprecedented rates, to help achieve worthwhile objectives such as education or decision making? Even though we are still witnessing such a revolution, we can already see the frustration and perhaps even the futility of our inability to cope with the information bombardment. We find that it is far easier to create and propagate information than to communicate effectively. This difficulty is shared by all institutions and individuals, and the US Army, whether in battle or not, is no exception.

In this paper we shall briefly examine three problems in the communication of information, one of which is nontechnical. First we will present a short summary of what communication and information technology seems to be offering over the next five to ten years. Then we will look at the difficult problems of standardization and information assimilation. Finally we will postulate an apparent contradiction in the broad dissemination and wide accessibility of information, and a rigid hierarchical command structure.

Because of the possible breadth such a discussion could assume, the scope here will be limited to the distribution of digital information.

The Offerings of Information Distribution Technology

-Computation

The heart of the information revolution to date, the driving force, has been hardware. Higher and higher performance and decreasing costs

have provided extraordinary opportunities to the weapon-system designer, to the information processor, and to the communicator. Capabilities in cpu power, size reduction, and memory continue to increase exponentially (Ref. 1; see Fig. 1). The 1980s will almost certainly see the million-component chip, the million-bit memory chip and the million-instructions-per-second cpu chip. Moreover the costs of these capabilities will approximate the level of today's microprocessors.

Of course speed, size, and memory capacity, even at low cost, are not in themselves sufficient criteria for a militarized computer. Other important trends in computation technology are listed in Table 1. Much will be offered and each item will have an impact on military systems. However several areas, such as distributed-system software, multiprocessor systems, higher-level programmability, and better, cheaper input/output devices, will move more slowly.

Table 1

NOTABLE TRENDS IN COMPUTATION TECHNOLOGY

- Increase in components per chip
- Increase in memory bits per chip
- Increase in cpu instructions per sec
- Increased parallelism for computational power and reliability, including fault-tolerant architecture
- Specifiable and verifiable software, including provably secure software
- Intelligent programs, including higher-level languages and natural language interfacing
- Increased computer networking

-Information Storage and Retrieval

The optimistic prediction of primary memory capacity, at least of the semiconductor variety, has already been mentioned. Secondary memories will also continue to increase in capacity and at correspondingly lower cost per bit and probably lower access time. But pure capacity is only the first step, and perhaps the simplest, in data storage and retrieval.

Other important attributes of storage subsystems are access time, error correction, non-volatility, low power dissipation, and a capability for associative access.

Of course only a part of the data-processing or information-processing systems important to the Army are data-storage-dominated. But those intended to support operations centers at the higher command levels, such as Division and Corps, are. Large data bases present not only access time problems, but may also suffer from a possible lack of data currency. One can conceive of intelligent memories that can insure the correctness of a read, and even reorder its contents so that more frequently accessed segments are made more readily available.

Other conveniences, such as natural-language interfaces, are now under development. They will enable the user to query the data base with a more normal, even conversational syntax. Many of the Packet Radio demonstrations conducted in California at SRI International used an intelligent natural-language interface to access a large data base in Boston.

Distributed data bases, including the software serving them are still difficult to develop; problems involve updating and concurrency.

-Communications

The same phenomenal growth in microcircuit capability that has revolutionized the computer industry has also benefited the radio industry. Size, weight, and power consumption will continue to decrease, and very simple receivers-on-a-chip are possible. Other devices, such as surface acoustic wave filters, also are contributing to receiver miniaturization, AJ/LPI protection, and reliability. Microcircuit frequency synthesizers with rapid and broad, but accurate, tuning are making jam-resistent frequency-hopping transmission practical.

But there are, of course, problems. While most designers rush toward the use of spread-spectrum modulation, few have adequately looked beyond the advantages to the susceptibilities such systems have. Their broad bandwidths make them more vulnerable to strong undesired signals, and occasionally to other identical radios in close proximity if the spreading codes are not sufficiently orthogonal (the near-far problem).

Network management is another common problem. This need is particularly acute in digital systems where operation of the subnet is intended to be automatic. It is clear that the higher echelons command centers must become more distributed and more mobile. There is not time to string wire, or install and align microwave systems. Omnidirectional antenna coverage and network self-organization and management should enable rapid deployment and mobile operation.

Probably the best embodiment to date of this automatic management capability is the Packet Radio concept developed at ARPA (Ref. 2) and now being introduced at Ft. Bragg by ARPA and CORADCOM. Packet Radio is a microprocessor-based, area-coverage, digital radio system now in the experimental stage. It provides end-to-end data services with high reliability and flexible topology. Its present configuration is shown in Fig. 2, and a program to reduce this size to about 30 cubic inches is under way.

There is one final note on the impact of technology. The sword that helps cut this mighty technological swath has a second edge. Some aspects of that other edge are shown in Table 2. Note that the items on the right are disadvantages only if the design, development, and procurement cycle is not well managed. More freedom and flexibility in design often require greater attention at the system level, or wherever two systems must join.

Table 2

THE NEW TECHNOLOGY: THE GOOD AND THE NOT-SO-GOOD

Rapid Evolution - Greater potential, sooner	Early Obsolescence - Shorter write-off period and higher cost - Technical improvement cycle shorter than procurement cycle
Broad Flexibility in Hardware - Easier, faster hardware design	Proliferation of Incompatibles Hardware - Interface problems
Flexible Software Design - Easier implementation	No Software Standardization - Little software transport

Lack of Standard Data Structures and Interface Conventions--- A Tower of Babble

Military communication literature has referenced the results of recent studies which delve into the lack of a unified approach to data communications in the battlefield. The present situation does not appear particularly good. (But hopefully not as bad as in Fig. 3!). The Battlefield Automation Management Plan (BAMP) study reveals more than seventy systems in various stages of completion that need data interconnection (Ref. 3.). Reportedly sixty-six percent of the problems in operating these systems involved the inability to move information from one processor to another. In addition, the required speeds (delivery time and data rate) are orders of magnitude greater than and fundamentally irrelevant to earlier traditional measures. As General Hilsman points out, "The precedences of the past don't make any sense when we move to this kind of information" (Ref. 4). For example, the vast majority of the nearly 50 targeting systems now under development require data transfer speeds of less than 15 seconds (Ref. 5). The sheer number of processors is also becoming important. By 1985 well over 600 processors will be operating in a fielded Corps (Ref. 6). Most

of these will have some communications need. Programs like CORADCOM's Military Computer Family are needed to help limit not only the needless proliferation of different computer hardware and languages, but also the number of different interface specifications (Ref. 7).

The Army has been blessed with new weapon systems capable of increasing the force multiplier necessary to bring us into parity with the enemy's greater numbers. Unfortunately these weapons systems seem to have evolved more or less independently; they either try to use existing communications equipment which was never designed for digital data, or they ignore communications and other weapon systems altogether. The results range from marginally acceptable to disastrous.

Let's look for a moment at TACFIRE--a system designed to use modern computational power to increase the effectiveness of field artillery. Forward observers or other target selectors must be able to communicate their designations quickly to the AN/GYK-12 at the Fire Direction Center, which subsequently interfaces with the battery computers that, in turn, program the individual pieces. The communication medium is VHF FM radio. Several frequency-separated nets exist, no protection against voice interference is guaranteed, and limited radio range rather than artillery range often constrains the distance the artillery can be to the rear. (By the way, that's not an advocation for more powerful radios).

Figure 4 illustrates the configuration at the AN/GYK-12, using the FM radios and necessary interface devices. The three IOX channels require seven radio and wire nets. The same computer interfaced via a host interface unit to a packet radio has the configuration shown in Figure 5. Not only can the interfacing be simpler and cheaper with a digital data concept as Packet Radio, but such a system offers the other advantages listed in Table 3.

With such studies as BAMP and the Army Battlefield Interface Concept, aggregate data needs and implementation concepts should emerge. Integrating approaches are definitely needed for the pre-INTACS period prior to 1985-7, the INTACS (update) period of the late 1980s, and beyond 1990. While communications alternatives, such as Packet Radio, JTIDS, or others, may solve part of the problem, it is important to begin with the data volume, rate, structure, and delay requirements of each system to be served. These requirements must then be made broadly compatible with the communications network. In turn communications systems should of provide throughput, delay, area coverage, ease-of-deployment, and flexible interconnect capability as good as the technology and available cost can allow.

But perhaps most importantly there should exist a flexible integration concept between the data terminal equipment (including host computers) and the communications medium. This could take the form of a clearly defined, structured set of communications protocols that extend from the electrical level up to and including user-user level. The design should require that any protocol level create a transmission medium that is as transparent as possible to higher levels. This

feature would permit the clean detachment at a layer and the substitution of a new transmission medium without delving into wholesale rewrite of the subscriber unit software.

Table 3

DATA NETWORK COMPARISON (Ref. 8)

	TACFIRE	PRNET
Network Organization	Imbedded communications software - Uses subscriber cycles - Requires other network elements	Essentially subscriber software independent
	Fully connected net - No relays	Relay allowed
	Total encryption Seven separate nets	Header in clear text One net
Network Monitoring and Management	Manual preconfiguration and monitoring	Automatic configuration and self-adapting
Architecture	Half duplex	Full duplex
	Character-oriented	Binary, bit-serial
	Manual access plus hold-off timer	Automatic carrier-sense access
	No routing	Routing
	Three-tier error control	CRC plus retransmission
	Narrow band	Spread spectrum
Communication Protocols	Retransmission	Retransmission
	Positive acknowledgement	Positive acknowledgement
	Limited msg. ordering	Sequencing of msgs.
	Unspecified duplicate detection	Duplicate filtering

Can't handle out-of-order msg.	Handles out-of-order msg.
No pipelining	Pipelining
	Software checksum
	End-to-end flow control

The Movement and Assimilation of Information---Doing Office at the Battle

It has been said that battlefield automation is the tactical Army's counterpart to the office of the future. But, as in the office, the generation and rapid flow of data around a battlefield doesn't constitute communication. At least half the communication process is receiving and filtering the information you believe is of use. This filtering is essentially in multiple-access networks but it maybe important in any network serving rigidly hierarchical organizations. Failing to realize where information should and shouldn't be available can lead to a misuse of the technology (see Fig. 6).

For example, let us assume that the Company commander has less need for information than say a Corps commander. His information is at least, of a different, less global type. Therefore the company commander must not have the same data base access prerogatives as do higher echelons. That restriction does not necessarily imply separate data bases for each level of command, although it might. Too much centralization of information, of course, creates a vulnerability.

Deciding on such prerogatives is a matter of command doctrine and must be dealt with in conjunction with the introduction of the technical capability.

Issues of this type can and should be explored and even experienced prior to a full scale development. Modern data communications and distribution capabilities are just beginning to gain some military exposure. A collaborative effort at Ft. Bragg between DARPA, various Army TRADOC organizations, CORADCOM, and the 18th Airborne Corps is intended to explore issues of this type. Some 40 data terminals will be distributed along the vertical organizational cut shown in Fig. 7 (Ref. 9), and individuals are being trained in their use. The terminals, both CRT and hard copy, are commercial grade and are linked through the ARPANET to a host computer in Los Angeles. The objective is to provide the technology necessary for exploring the replacement of some of the present manual reporting with on-line, real-time access. The initial installation uses wire access to an ARPANET Terminal Interface Processor (TIP) located at Ft. Bragg. Some of the on-line functions developed in garrison will be taken to the field in 1980 using a packet radio network that is already on site. Figure 7 represents one alternative deployment. A list of candidate reports to be "converted"

in such field exercises are shown in Table 4 (Ref. 9). These reports have been selected after considerable discussion with Corps personnel.

Table 4

CORPS ELEMENT REPORTS

Reports	Frequency of Issue
Operational Reports (G-3)	
Situation Reports	12 hours
Unit Location Update	4 hours
Logistics Reports (G-4)	
Logistical Status Report	24 hours
Battle Loss Report	24 hours
Intelligence Reports (G-2)	
Spot Intelligence Report	As required
Intelligence Summary	24 hours

In addition, special programs have been written, such as one to query up-to-date weather forecasts. Many of the services normally available from ARPANET hosts, such as electronic mail and text editing, are also available to the new users.

At the moment, data represents no more than a few percent of the total battlefield communications traffic. CACDA favors both voice-data integration and the increased use of data at all levels, but with voice continuing to dominate the echelons at Brigade and below. For these and for reasons cited earlier, the trend to data traffic will increase significantly in the next decade; this will not only come from the increased use of digitized voice, but also from the wider use of data in both information service-systems and weapon systems. Communications equipment must change to permit that transition.

We find our communications development in a serious time lag situation. INTACS-specified hardware will probably not appear before 1985 at the earliest and furthermore, nothing is available to meet the data distribution requirement in the interim. That condition ought at

least motivate us to use this period to determine how a new and flexible distribution system can be integrated into our present communications inventory and what impact it will have on organizational structure and mission. We will now mention one aspect of the latter question.

Distributed Real-Time Information and the Hierarchical Command Structure

As a final point I would like to raise a purely nontechnical issue that is precipitated by the very technology we have mentioned. The issue will certainly become a problem if it is ignored in the design of information distribution systems. It may remain a problem even if it is considered. (By the way, the issue is not that the commander wants to hear a voice). To illustrate the potential problem, I will first make the assumption that an idealized information distribution exists; one that satisfies all the major battlefield requirements. Rapidly deployable area-coverage communications, and readily accessible, topically structured data bases with natural language interfaces provide the commander with instant information about the subject of his choosing. Assuming that the various weapons, intelligence, and logistics systems all have their communication needs met, the commander now has much of the force multiplier that is the broad objective of such technology. What then?

The next step is the very difficult problem of controlling the vertical flow and content of information in the organization. From this issue a couple of important questions loom out at the designer:

(1) How should the information available at a given command level be meted out to subordinate commanders?

(2) How clearly should a given commander be able to probe the information detail found at levels two, three or more echelons below?

While I'm sure the TOS designers have struggled with them, let us look at each of these questions briefly.

Obviously, matters such as the privacy and security of information are command prerogatives. The transfer of total information to a subordinate is likely only with transfer of command. But if, as some assert, the increased reliance on data bases may cause a corresponding decrease in reliance on staff, the assumption of command may be harder to deal with under the new technology. For example, suppose a Division commander and some of his key staff are killed. One of the keys of the assumption of command is the right of data base access appropriate to that level. Who is the keeper of those keys? The residual staff? The next higher commander? What if they are not available? Suppose the designated Brigade commander can't or does not choose to relocate and, therefore, must access the information remotely? How are the data and access privileges assumed? These questions are not imponderables but they do require study and resolution.

The second question has an interesting corollary: What freedom does a subordinate commander have, if any, in limiting the amount of traffic he contributes to a centralized pool for a higher command level? In other words what insulation does lower echelon commanders have in this new relationship? Should a Corps commander, for example, be able to query information sources at the Company or Battalion level? If so, can (should) it be done without the knowledge of the responsible commanders along the chain of command? Present computer and communications technology makes it possible for a commander to know with unprecedented currency and detail the status (presumably accurate) of the resources under his control. What does this do to the discretion of subordinate commanders. Will instant probing of battle fitness and the consequent *susceptibility to being* micro-managed cause the subordinate leadership to see their roles emerge to that of information gatherers? The impact could be devastating. The potential is there.

To appreciate the extent of the capability sought, consider, for example, the Battlefield Exploitation and Target Acquisition (BETA) Project. BETA is an automation program intended to aid NATO commanders in learning of enemy forces. An objective is to keep track of 500 enemy command posts, 1,000 air defense units, 1,000 artillery batteries, and 3,500 multichannel and push-to-talk radios. Sensor reports may total 7,000 reports per hour (Ref. 10). Add comparable numbers for the friendly forces and you have a formidable data collection and presentation problem. But with available technology a commander, charged with the broad responsibility such forces imply, can still zoom in on the position and status of a platoon or company. Resisting the temptation to manipulate resources at the lowest levels represented in the data base will take considerable restraint.

Let me close with a little anecdote that relates not to the way on which a commander provides information to his subordinates but how freely such data can flow in either direction without explicit constraints. During the course of instruction for the GIs at Ft. Bragg on the use of the new computer-based message service recently made available to the 18th Airborne Corps, one student obtained from the system the names of individuals who had mailboxes. During a session on creating messages, the student blurts out, "Hey, who is this guy Starry I just sent a message to?" Answer: The Commanding General of TRADOC. Gulp!

Conclusions

While this paper has mentioned some of the problems inherent in information-distribution technology, we wish the overall impression to be emphatically positive. Digital data systems must be available as soon as possible for essentially all military functions from command and control to air defense artillery. While it is possible that no one data-distribution system may be able to satisfy the wide range of Army needs, seeking one should receive our best effort. Reliability, modularity for replacement and expansion, flexible interfaces to

terminals, hosts, and other networks, and subscriber-defined transmission characteristics are not as utopian as they may first sound. There are pitfalls and we have mentioned a few here. But a solid commitment and quickening the pace of our search are very much in order.

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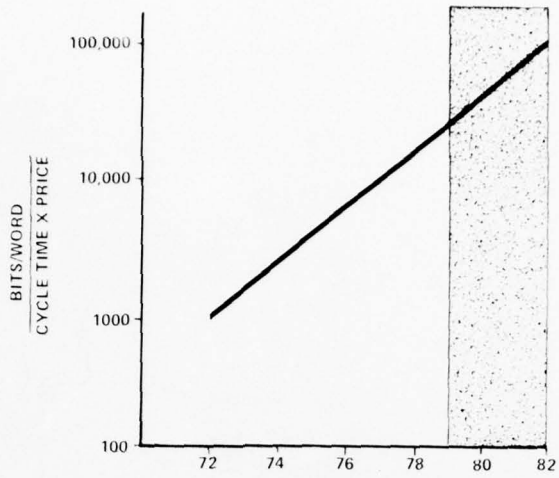

Figure 1 Performance Trend for Microprocessors

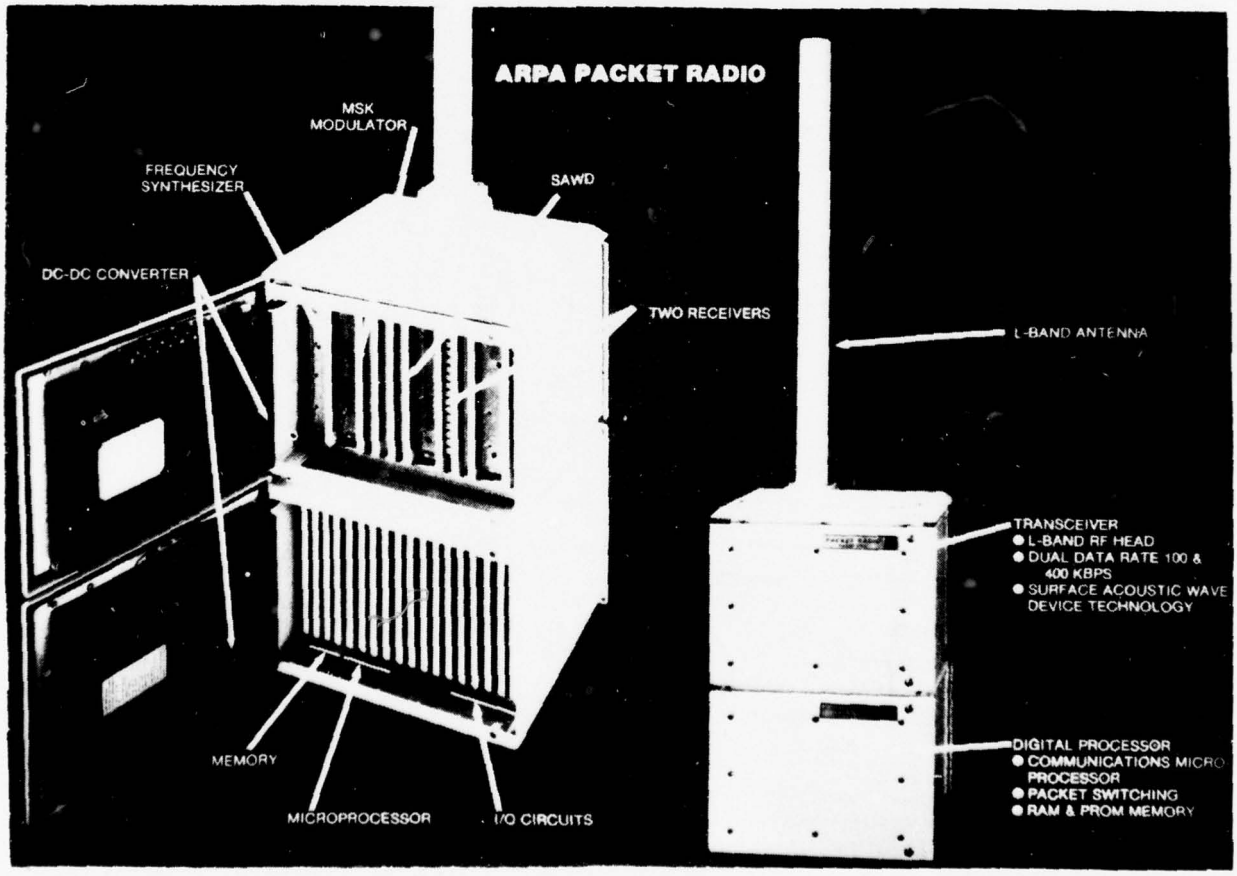

Figure 2 Experimental Packet Radio

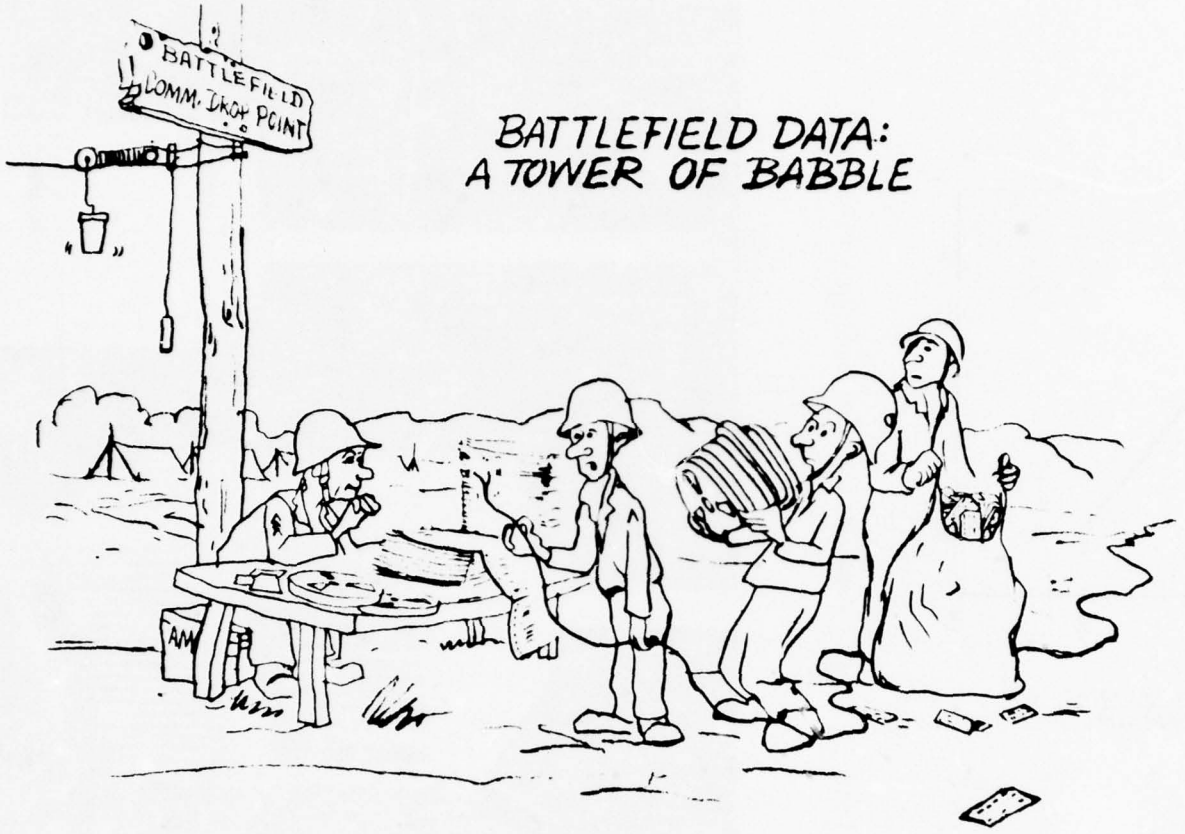

Figure 3 The Battlefield Data Compatibility Problem Exaggerated

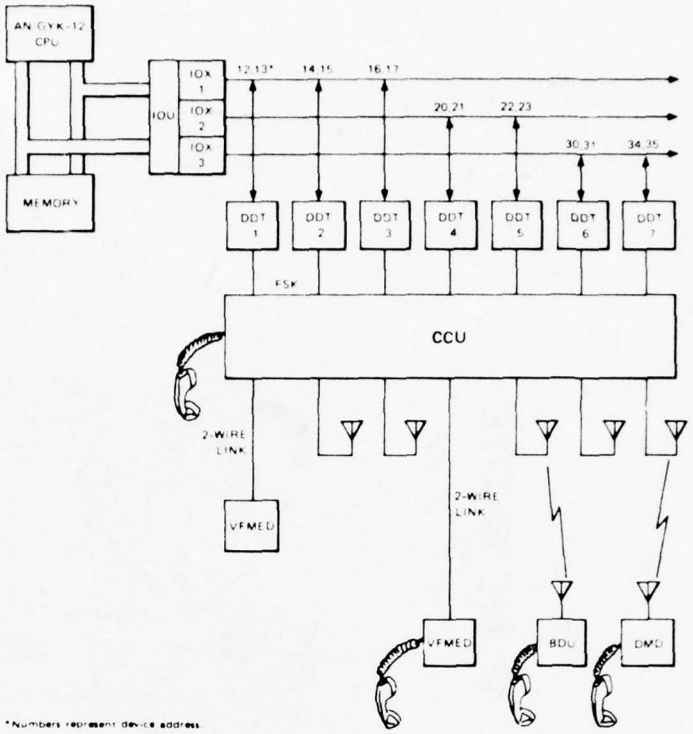

Figure 4 Typical AN/GYK-12 TACFIRE Communication Configuration

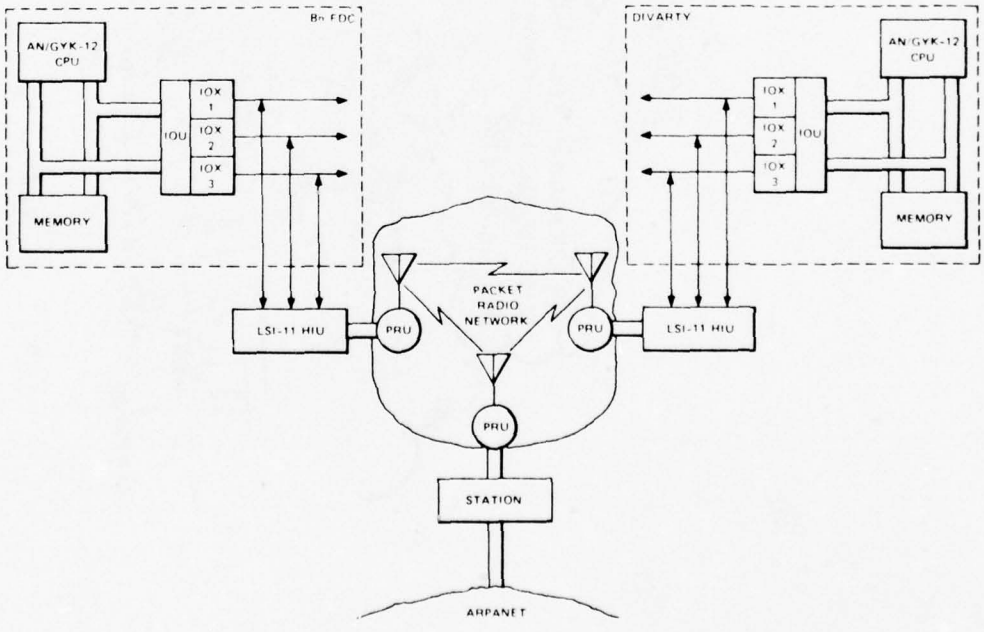

Figure 5 Proposed TACFIRE Communication Configuration Using a Packet Radio Network

Figure 6 Doing Office at the Battle

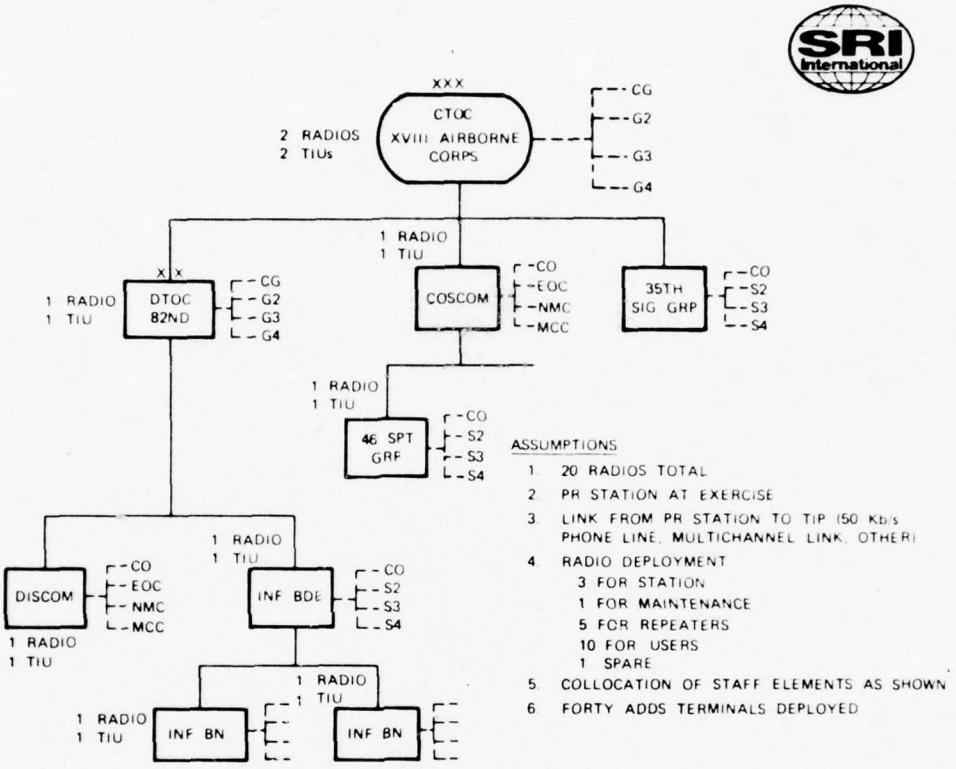

Figure 7 Proposed Deployment of the Packet Radio Equipment in the Ft. Bragg Testbed. (Station is the packet radio control node and a Terminal Interface Unit (TIU) interfaces a packet radio to a data terminal.)

TECHNOLOGY INSERTION--TRAINING DEPENDENT

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The application and introduction of significant technological change in Army systems must consider the total man-machine interface. The ingenious work of scientists and technicians in the research and development community will ultimately be doomed to failure unless there is an awareness of the Army's capability to operate and maintain new hardware and systems. This Army capability translates to people and the actions of recruiting, training, assigning, and retaining qualified soldiers. Each of these functional areas presents sets and subsets of unique problems that the scientists and materiel developers must consider. This paper will focus only on one aspect of the total people-machine system...training.

THE CHALLENGE

A highly sophisticated piece of equipment or an equipment modification processed through the materiel acquisition cycle may use the very latest state-of-the-art technology, but its complexity may prevent optimal training for the average soldier provided by society. As a result, maximum utility may not be gained from the equipment. The training challenge is to insure that the typical soldier can be trained to operate and maintain the latest adaptations of science in Army systems

and hardware. This challenge is met in the training development community by properly establishing tasks, conditions and standards for operators and repairers, developing and validating training materials, then confirming that the necessary skills are acquired. The trainers, from schoolhouse to the company motor pool, deliver training. Roger's Rules for Rangers called for rehearsals and training; the calvary soldiers spent endless hours practicing formations and movements for combat. Today's Signal Soldiers are no different...their school training, exportable training, and unit training is rehearsal for combat. When changes occur, the soldier must be trained to use the applications of technology effectively.

THE AUDIENCE

A brief look at the training business is necessary to understand the bounds of the challenge. The US Army Signal Center, Fort Gordon, a subordinate activity of the Training and Doctrine Command, is responsible for developing and implementing training, both resident and exportable, for the Army's 110,000 communications-electronics officers, warrants and enlisted personnel. This group is a diverse mixture of operators, maintainers, and managers who serve from the White House to the foxhole. In the enlisted ranks, there are currently 51 military occupation specialists (MOS) in five Career Management Fields (CMF) which comprise 151 skill levels. Three commissioned and two warrant officer personnel management specialties are also our responsibility. All of these Signal

Soldiers, as well as the training developers and trainers, are affected by today's exploding technology.

THE METHOD

Upon enlistment, the Signal Soldier receives institutional training on the most critical tasks of his or her MOS. Following initial training, the soldier is assigned to a unit where the training is continued using formal training support products, such as, Army Training and Evaluation Program (ARTEP), Soldier's Manuals (SM), Training Extention Course (TEC), Army Correspondence Course Program (ACCP), and field and technical manuals. Skill Qualification Tests and Army Training and Evaluation Programs verify that the individual and collective combat missions can be performed. Because these training support materials usually describe the employment, operation, or repair of more than one type of equipment, a single product improvement or new equipment introduction will change many training products. Each of these products has its own development or revision cycle. It is important to understand that changes in training requirements will affect multiple resources in the support base and the field.

RELATIONSHIPS

As discussed, training the soldier is a continuing process encompassing both resident and extension training. The essential ingredient to effective training is a comprehensive training package; this brings us to the training development process. The training developer analyzes, designs, develops, and produces the training materials for world-wide

distribution. The life cycle management model recognizes the need for the close interrelationship between the materiel developer and the training developer for new systems and subsystems. In fact, the Skills Performance Aids (SPAS) program specifically addresses this need for developing systems or equipment. It is absolutely critical for training development to be in close coordination with materiel development of product improvement packages. The time required to do job/tasks analysis, design, validation, development, production and distribution of training materials dictates early involvement to insure a synchronized development effort. The bottom line, as stated in a special 1979 Office of the Secretary of Defense study, is that training development needs to be an integral part of the research and development process. The Skills Performance Aids program is a major step in meeting this need. Currently, the training development function is done in each of the Training and Doctrine Command schools. It is resource intensive. For example, the FY-80 training development workload at the Signal Center translates to almost 1,100 validated manyears of work. Of this total, 78 manyears should be devoted to tracking and integrating new equipment, systems and hardware. The work force dedicated to this function follows a systematic process of analysis, design, validation, and development against tasks, conditions and standards for the 51 MOS, 151 skill levels cited previously. Experienced subject matter experts in each MOS, complemented by educational technologists, testing psychologists, and training managers are required to engineer the training materials. The introduction of higher

technology via product improvement or new systems necessitates a significant and expensive training investment in order to qualify the training developers to make informed decisions on the training process. Training decisions cannot, however, be made unilaterally. Relationships must be established and input obtained from every Army activity sanctioned to insure that systems or equipment are successfully fielded.

ANALYSIS

A mutual understanding and appreciation of the roles and functions of the key players in new equipment/hardware is essential. A brief description of the training development functions and its relationship to the technology insertion process will clarify the interrelationships. What is the Training Analysis function? Basically, the function involves analyzing the proposed change in terms of the effect on the operator, maintainer, and manager of the equipment being changed. This analysis answers the questions concerning the soldier's tasks--What is new? What requires modification? What is eliminated? Do the new tasks exceed the capabilities of the assigned operator or maintainer? Do the new tasks change the criteria for an entry MOS? Additionally, this function incorporates the writing of the task statements which identifies the job of the soldier. To be effective, it is essential that any training analysis proceed simultaneously with the materiel developer's analysis of technologies being considered for fielded systems. In fact, training analysis must be a major consideration in the decision process for technological upgrade.

DESIGN

Upon determination that revision or addition is necessary, the design function of the training developer becomes important. Using the results of analysis, the training developer designs a training package to provide for new or modified tasks. The design phase incorporates a critical event called site selection; a determination of whether the training should be conducted in the resident mode or exported to the unit, or a combination thereof. A determination is also made concerning media for the training package and if existing training support documents can be modified or new materiel must be developed. As we move into training of embedded processor-driven systems, the software packages become inportant elements in the design process. If coordinated and executed properly by materiel and training developers, the software programs can have application both in training and in on-line operational use.

DEVELOPMENT

The development function is the "nuts and bolts" of the implementation of the training changes caused by equipment alteration. Specific modifications to Programs of Instruction (POI), changes to ARTEP, Soldier's Manuals, Job Books, Commander's Manuals, TEC, ACCP, and Skill Qualification Tests (SQT) primary to products, are necessary. The principal action, therefore, represents a complete, comprehensive, consistent training package. This training package must be synchronized with the change formulated by material developers and cyclic revisions to

individual and collective training material. The publication and distribution of training packages is primarily a mechanical function but should not be overlooked. Sheer volume may preclude a reasonable fielding of any changes.

COORDINATION CRITICAL

As indicated earlier, materiel developers, training developers, and trainers must, by necessity, become involved in the personnel management business. As technological improvements to systems and equipment are made, there is a subsequent impact on training, which will impact on MOS criteria, which impacts upon force development, personnel management, and eventually upon recruiting. The ripple seems endless but the mechanisms and systems are available to properly handle the impact. Awareness and use of the process in a timely manner is paramount.

Technological progress is a way to enhance the Army's capability to accomplish assigned missions. To maximize the benefits of technology, the soldier must be trained. Proper training of the soldier can only result from effective working relationships of the materiel developer, the training developer, and the trainer. Technologically superior systems in the hands of qualified and trained soldiers is an investment in preserving the peace.

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A MAINTENANCE PROSPECTIVE OF TECHNOLOGY INSERTION

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Before I embark into the MULTI-FACETED Impact of "Technology Insertion" on Army Maintenance, I think it appropriate and necessary to set the scene, the program scope, the today aspect of where we are.

FIRST TECHNOLOGY

We know that technology is experiencing a growth rate which far exceeds anything which has occurred in the past. This growth in new ideas, techniques and capabilities is being rapidly applied by Industry to its products. The translation between discovery, application and hardware/software is the hands of the industrial user is defined in years and some times in months. One part of this growth is not, however, well defined; osbolescence.

The availability of parts, assemblies and even equipments of a specified design in this market place is limited by the industrial adjustment to technology growth. This adjustment is dictated by economics and is both effective and efficient from a producer viewpoint. It is, however, a potential maintenance nightmare. Equipment which performs well, does its job but cannot be either repaired at all, or economically repaired, due to its parts/components being obsoleted by technology change, is becoming a major consideration in maintenance decisions.

We have choices - modify the equipment via technology insertion, shorten equipment life cycle or plan and implement support early. Actually, all courses are currently being pursued.

The first two approaches represent technology inseration from a system viewpoint. Selection on one over the other is a matter of economics. We, in Maintenance, are familiar with technology insertion to a very limited degree strictly for maintenance needs and to a greater degree for an increased equipment capability; product improvement modifications. But we realize this is only the tipe of the iceberg which is approaching.

To assess the impact of technology insertion on Maintenance, it is necessary to understand the Army Maintenance Philosophy, Policy, Program Size, Elements and Status of Ongoing Operation; the bounded rationality in which, and from which, we must operate. We will bear briefly with the elements listed below.

Army Maintenance Philosophy is in simple terms as stated here.

ARMY MAINTENANCE PHILOSOPHY

* Maintenance is a command responsiblity
* Maintenance is accomplished at the lowest level
* Unit commanders must have a reliable and responsive maintenance source

The last two stars are those which must be considered in assessing the impact of Technology Insertion.

The Army Maintenance Policy is deliberately structured through Logistic Support Analysis to achieve maintenance at least costs for a required mission profile. Field readiness is our guiding principal.

The annual cost of maintenance in the Army represents Big Bucks as shown here.

MAINTENANCE - BIG BUCKS

(FY 78 PROGRAM)

Overhaul/Rebuild	$1.0 B
Post Shops	.3 B
Field Units, ARNG, USAR	3.2 B
(People and Materials)	
TOTAL	$4.5 B

And we are striving to get more bang out of these dollars spent.

From a system viewpoint, the principal elements of maintenance are as depicted in Figure 1. In assessing what Technology Insertion could do for us or to us, we must, in essence, evaluate the logistics factors of maintenance; they are the same as the factors of production which industry must consider in its business.

To set the scene fully, we must at least mention that there are in program programs to upgrade the Army Maintenance Program. This involves an attack on the element listed above with the aim to Better Force Readiness at minimum cost.

Reliability Center Maintenance - another initiative. Because reliability and safety are design parameters and can only be enhanced through design changes, the most that can be expected from a Maintenance Program is the preservation of these design parameters. RCM is a technique to logically determine the optional scheduled Maintenance Program which

will preserve reliability and safety levels and do so with minimum maintenance burden on field personnel. This technique considers equipment functions, failure modes and failure effects.

Figure 2 is presented to give you a feel for the length of time an item of equipment is in the Army system. We can from this predict that the life cycle reaches more than 30 years and that usually there are two or even three generations of equipment out there for the same job. We are looking for means of improving this situation, but it does give a parameter that must be taken into consideration in technology insertion.

Having set the scene, let us examine technology insertion as it impacts on Maintenance from the aspect of Army Philosophy considering the elements previously outlined. We must, however, not forget that Technology Insertion has in todays connotation certain inherent benefits:

a. Greater reliability giving longer periods between maintenance actions and the potential for economic throw away.

b. Reduced size and weight making practical redundancy and BITE.

c. Micro processors, etc - giving rise to smart machines.

These and other innovations such as ROM, LSI, Etc., present the potential for maintenance simplification never realizable before. And such advantage poses a unique challenge to the logistics system in terms of timing, concepts and the new hardware - computer software.

In the R&D cycle, technology growth frequently dictates changes to materiel up through initial production. Yet to implement our maintenance philosophy, to have a reliable and responsive maintenance source, we must

plan and develop our logistic tools during this period if we are to be ready to meet the unit commander's need at deployment. This required a system and concept geared to change. This change, however, must be transparent or invisible to the man in the field and to the system which implements it and yet must still guarantee field readiness. This leads to the impact of Technology Insertion on maintenance.

IMPACT ON MAINTENANCE

Timing then becomes a crucial impact. Some of consideration we current have under advisement appear to offer hope in this area.

Provisioning of Repairable Only Utilization of Contractor/Depot repair for 1-2 years. Pushing Maintenance forward based on experience gained during this period in order to meet the Army philosophy.

Again, however, we must be aware of the Beast of technology growth, obsolescence, and must have the management tools to evaluate the need for such things as parts buyouts, plan component conversion, etc.

Technology offers through its size and weight reductions the potentials for throw away, redundancy and BITE which was not previously possible. The potential for throw away will reduce the impact of technology growth by allowing Technology Insertion via modules. Redundancy will permit repair without part stockage (i.e. a self-repairing instrument) and BITE will speed up the identification and location of a failure. It will also simplify the interface between the instrument under test and its test equipment.

In supporting equipment in the field, it is essential we supply the operator and maintenance personnel with technical instructions - on the equipment - the Technical Manual. As long as the Technology Insertion is transparent to the field, this type software, at least for the operator, and lower echelons of maintenance should require little revision. Higher level maintenance documentation should change and we must structure to accommodate this change. The timing discussed previously, will help in the initial deployment. Insertion after deployment will involve some changes and these type changes must be planned for both in the management sense and in the conceptured structure of the software.

Computer software and its maintenance are the major challenge of the new technology. This type software presents a new dimension in Technology Insertion as well as a new discipline in maintenance. The software used in the field for operation and self-diagnosis requires change not only to eliminate problems/errors but also to supply new capabilities. It will also change as we insert new technology into hardware through product improvement. It has a further dimension when we consider that current assessments dictate the use of ATE to perform, as a minimum, higher echelon maintenance on these items. Here we have the potential for Technology Insertion via software for maintenance purposes.

Blending all these elements together into a cohesive, effective and economic maintenance plan for the Army is the challenge.

We must organize the elements of support for change (i.e., the TMs, Parts Lists, Tools & Test Equipment). We must structure these elements

in such a manner as to permit change easily and economically while still supplying the necessary information to the field.

Secondly, we must change our approach to support so the timing is such as to permit adequate and require data to be available without impacting on field readiness.

However, the biggest challenge is to plan for change, not just to incorporate it in the field but to forecast change and use this forecast as the management tool to take technology in appropriate BITES. Delay development where major technology change can be predicted. Insert technology into equipment when it has a potential for limited stability/ It is further incumbent on us to make Technology Insertion as transparent to the maint in the field as possible. To incorporate technology in such a way as to minimize its visible impact on the operator and maintenance personnel. To accomplish this, it is essential that the Technology Insertion be designed to blend with existing field support. This places a responsibility on the designer to be aware of the coordinate with the Maintenance Engineer. To go one step further, the initial hardware developed, should consider Technology Insertion, and be designed to be ready to accept such insertion (i.e., Technology sensitive areas should be modularized).

In the manual area, the Army has established a working group to investigate automated text editing and photo composition. Should this prove feasible, we will have the capability to store TM data in a computer. This will speed up the ability to change technical documentation and will reduce its cost.

We have taken an initial step in this direction in our approach to TMDE in the Army and details on this are to be presented as part of the seminar for which this paper is written.

SORTING IT ALL OUT

Changes in Logistics

Timing

More throw away

Software maintenance

Planning for Change

Technology forecasting

Buy out of tech sensitive components shorter life cycles

Planned insertion

Discrete bites

Field transparency

Structure for Change

The above represents what i consider major points. These are a few I would like to discuss in more detail.

Technology forecasting is absolutely essential to any viable program. Without this all important tool, the planning ahead to utilize Technology Insertion or to avoid or reduce the impact of obsolescence through technology cannot be done on an intelligent and cost effective basis.

The structuring for change must involve the hardware, the software, and the organizational environment that implements Technology Insertion.

The gearing for change is as essential as the change itself. Our challenge in the Army is to gear for this change.

In summary, what we in maintenance really need is the best technology but with standardization. The best of two worlds.

PRINCIPAL ELEMENTS

COMMAND EMPHASIS

MAINTENANCE OPERATIONS

TRAINING

PERSONNEL

PUBLICATIONS, TOOLS, & REPAIR PARTS

FIGURE 1

AGING OF C-E EQUIPMENT

EQUIPMENT	ROLE	PERCENT FILL FUNDED IIQ	PERCENT FILL FUNDED AAO	YEARS FROM TYPE CLASSIFICATION TO ACHIEVE % OF IIQ SHOWN
AN/VRC-12	TACTICAL FM	100%	58%	19
AN/PRC-77	TACTICAL FM	100%	64%	17
AN/TRC-145	DIVISION LEVEL MULTICHANNEL	100%	64%	15
AN/MSC- 29/TSC-58	DIVISION LEVEL T/T TERMINAL	94%(50/44)	91%	19(19/7)
AN/MGC- 17/TGC-30	BDE LEVEL T/T SWITCH (CENTRAL OFFICE)	119%(94/25)	79%	20(20/8)
SB-611/AN/TSC-76	DIVISION LEVEL PATCH PANEL	100%(55/45)	96%	14(14/5)
AN/TRC-110	CORPS/ARMY MULTICHANNEL REPEATER	85%	71%	12
AN/TRC-117	CORPS/ARMY MULTICHANNEL TERMINAL	81%	67%	12

FIGURE 2

JAMES A. CARTER

Mr. Carter is the Chief, of the Electronic Equip Support Division, Maintenance Engineering Directorate, CERCOM. He has been in the Maintenance Business since 1963. Mr. Carter has a BS in Physics from Villanova University, Master of Science (Undesignated) in Industrial Engr and Mgt from Newark College of Engineering and a Master of Public Administration (MPA) from the University of Indiana. He was the recipient of a Scholastic Scholership to Villanova and was an education for Public Management Fellow at Indiana. Mr. Carter has 5 children, three boys and two girls. Two are married, one is in college and two are completing high school. His wife, Marigene, is considered by all a major factor in his life.

TECHNOLOGY INSERTION IMPACT

BRUCE LOWING

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US Army Communications and Electronics
Materiel Readiness Command and Fort Monmouth
Fort Monmouth, New Jersey 07703

The purpose of this paper is to present the logisticians view of the new "Technology Insertion" concept. It presents a general sketch of the impact on the entire logistics spectrum and provides specific recommendations to the repair parts managers.

First, let's discuss one way of defining Technology Insertion. It is a design methodology which allows an item of hardware to "easily" accept new technology over one or more future change iterations or technological generations. To the hardware designer it is a method of avoiding the "drawing board obsolesence" problem so prevalent in long lead time military communications electronics. To the logistician it is a method of avoiding the high cost of procuring obsolete parts of a past technology. It is also, however, only as good as our forcast of technology evolution.

At first glance, Technology Insertion is, to the logistician, just a bigger version of the old recurring nightmare of hardware change after design freeze. In the past this has meant things like "serial number effectivity" control of technical manuals, parts lists and, often,

training, all resulting in confusion to our maintenance and supply managers and to field maintenance personnel.

With a bit deeper reflection, however, perhaps Technology Insertion is not so bad. In the past the designer elected one of two options--he either designed an entirely new device (system, black box) or invoked a PIP. The former resulting in an entirely new logistics problem. The latter in an under-funded, hastily planned action with often spotty field application. Of course, we won't discuss the rare case where a change simply happened with no warning whatsoever to the logistician. Under Technology Insertion, change becomes a "way of life." Succeeding change iterations can be planned well in advance, allowing the logistician to interact with the designer in formulating and budgeting the change actions. Even when unplanned changes must occur, the fact that a planned change in "on the way" can only assist implementation (a budget exists, contractor assistance should be available along with an entire spectrum of ILS change actions already in being).

Now, what specifically must the logistician do to ensure that all of these good things happen. As is normal in logistics, let's look at the problem backwards, i.e.; look first at where we want to be, then at what we must do to get there.

At some arbitrary "insertion" in the future for a given item of hardware, we must be ready on a specific date with the changed hardware (and software) and a completely changed ILS package. The ILS package will

encompass Technical Manual changes (or revisions), new parts (fielded), training, personnel, TMDE, and possibly, Depot or contractor repair.

Prior to contracting for this, some tradeoff process must provide a final decision of precisely what design effort may take place. Inputs are budgetary restrictions, previously unforseen design deficiencies and technological innovations, maintenance concept changes, provisions for future technological insertion and, of course, the forseen and "inserted" technological innovations. In short, the same modeling/analytical/budgetary/execution process that generated the previous iteration and the original item.

As a corollary, there is no reason, in principle, why a Technology Insertion could not or would not be performed on an item originally designed without Technology Insertion.

One of the most extreme examples of what can happen in a "non-Technology Insertion" world is our own Tactical FM VHF radio, the AN/VRC-12 series.

Under Technology Insertion, parts obsolescence, both at the stock fund and the Secondary item levels are planned for obsolescence instead of the current "buy at any cost--as long as someone will make em" policy. It is in this area that our efforts must be expended in refining our logistics modeling techniques. Things like "Life of type buys" and "production life" analyses must come to be the forefront and, ultimately, drive the timing if not the fact of Technology Insertion.

There is, in fact, every reason to conclude that this kind of parts availability analysis and forecast technique should exist independently and permanently as a part of every communications-electronics readiness organization. How many times in recent history have we been "caught" unprepared when a seemingly common part is suddenly out of production like those parts in the VRC-12.

This cannot be a half-hearted effort. Establishment of a "production lifetime" on whole classes of parts should be undertaken and considered automatically in driving our provisioning process and the new Technology Insertion process.

How this can be accomplished organizationally is for management to determine. It must, however, be implemented within our CCSS supply computers and be driven by logistics engineering input.

This radio was designed in the late 1950's and fielded in the early sixties during a time when germanium transistors, tubes and mechanical gear trains were the best and only way to design a semi-automatic radio. During the long years of fielding, we watched germanium transistors go into design and production obsolescence to the point where the formerly common transistors in the VRC-12 are only in production to support our radio - at a fantastically high cost.

Finally, in 1979 we have approved new designs for a siliconized version of the VRC-12. Tubes and gear train remain unaffected by the new design. No study has been made on the obsolescence date of the new transistors or

what devices might replace them. Design guidance to the contractor was basically to replace the old items on a "one for one" basis with new devices. The radio has an estimated 15 years of additional service.

Under Technology Insertion, the radio could have been up-graded gradually through the years under a carefully regulated program to become almost the same radio we have been trying to design - the SINCGARS-V.

This tendency to "put out the fire" and solve immediate problems with no or little regard for the future is what the whole concept of Technology Insertion is designed to combat.

Enough, then, of a logistician doing "Monday morning quarterbacking" to design. What can the logistics community do to warn our brothers in the design community of impending disasters and generally assist the Technology Insertion effort.

First, of course, is the tradeoff analysis and programming effort mentioned earlier. The second thing however, is more intensive parts management. Our current attitude is that if we do not manage a part, we have no responsibility for the part.

In summary, Technology Insertion in the Readiness environment will revise the methods under which we perform tradeoff studies, increase the frequency of past deployment design changes and require more intensive parts management.

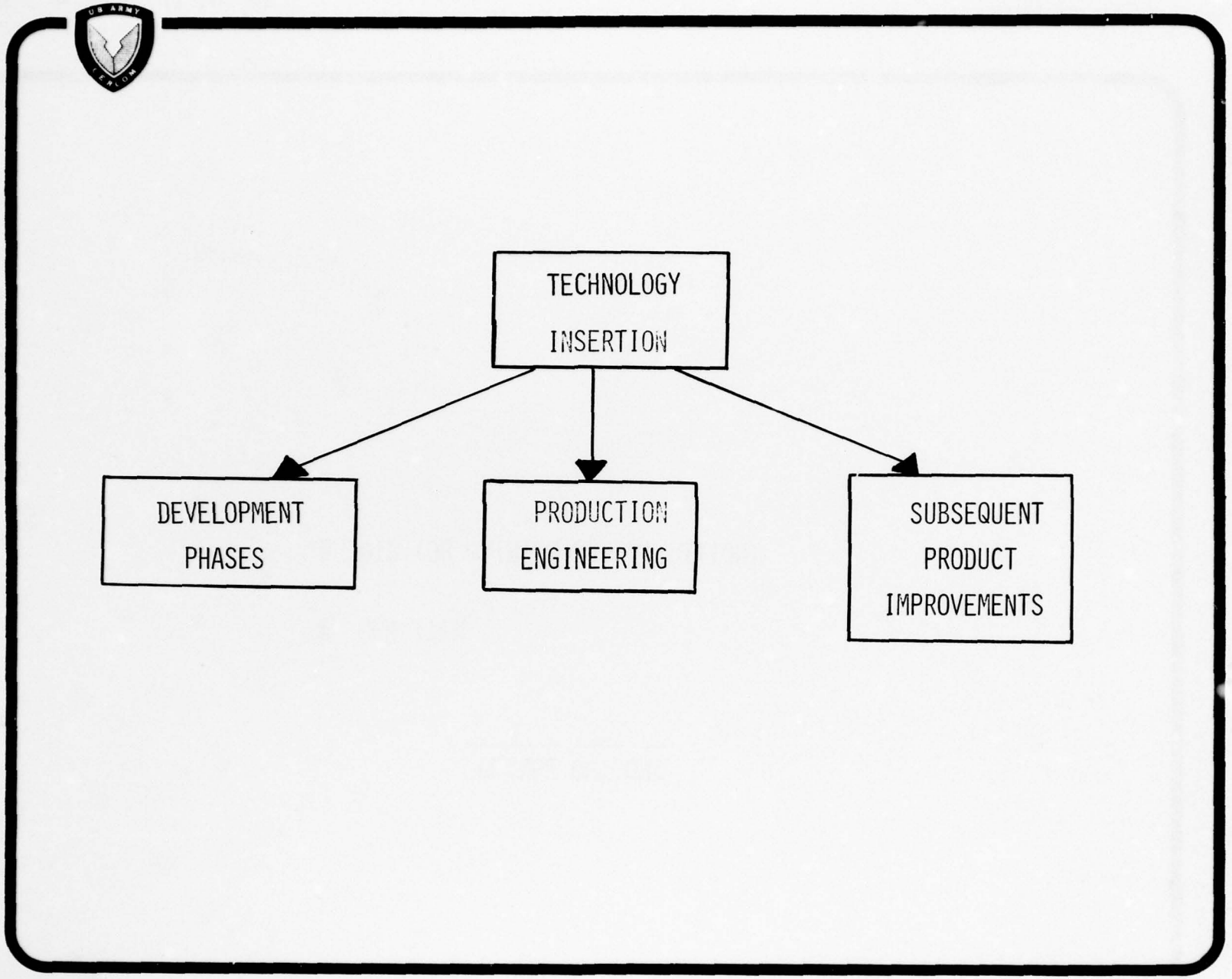
TECHNOLOGY INSERTION IMPACT

ON

REPAIR PARTS MANAGEMENT

AND

ILS


TECHNOLOGY
INSERTION
DEVELOPMENT
PHASES
PRODUCTION
ENGINEERING
SUBSEQUENT
PRODUCT
IMPROVEMENTS

CHANGE OPTIONS

☒ NEW ITEM

☒ PIP (OR MAINTENANCE ATTRITION)

ILS ELEMENTS AFFECTED

- ☒ TECHNICAL MANUALS
- ☒ REPAIR PARTS
- ☒ TRAINING
- ☒ PERSONNEL
- ☒ TEST EQUIPMENT
- ☒ DEPOT/CONTRACTOR REPAIR SUPPORT

TECHNOLOGY INSERTION INTEGRATION

TRADEOFF ELEMENTS

- BUDGETARY RESTRICTIONS
- UNFORSEEN DEFICIENCIES
- UNFORSEEN TECHNOLOGICAL INNOVATIONS
- MAINTENANCE CONCEPT CHANGES
- FUTURE TECHNOLOGY INSERTIONS
- PROGRAMMED TECHNOLOGY INSERTIONS

AN/VRC-12 DESIGN

- GERMANIUM TRANSISTORS
- TUBES
- MECHANICAL GEAR TRAINS

TECHNOLOGY INSERTION IMPACT

ON

READINESS MANAGEMENT

- CHANGE TRADEOFF STUDY METHODS
- INCREASE FREQUENCY OF POST DEPLOYMENT DESIGN CHANGES
- REQUIRE MORE INTENSIVE PARTS MANAGEMENT

BIOGRAPHY

BRUCE S. LOWING

Mr. Lowing received his BSEE from the Michigan Technological University in 1964, his MSEE from Fairleigh Dickinson University in 1971.

He currently is accumulating credit toward his MSCS at Fairleigh Dickinson.

He has been employed at Fort Monmouth since 1964 in the Maintenance Engineering Directorate and Logistics Engineering Directorate (ILS Management Office), U.S. Army Communications and Electronics Materiel Readiness Command.

Mr. Lowing is currently a member of the Office of the Command Manager for Initial Support (CMIS) but is on detail as Team Leader of the AN/VRC-12 Depot Overhaul Task Force at Tobyhanna Army Depot.

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